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Gain-Determined Short-Channel Limit of MOSFETs

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1. Introduction

Channel length of a MOSFET has been reduced to improve operation speed and integration density. Recently, fabrication of a 30-nm-channel MOSFET has been reported[1]. On the other hand, the prediction of sub-0.1-μm MOSFET characteristics also has been evaluated[2], where leakage and driving current are mainly paid attention to. Besides these current characteristics, active devices including MOSFETs in a logic circuit need to have enough voltage gain to restore a signal swing

In this report, short channel limit of MOSFETs determined by gain is studied. From the next section, after the relation between input-output characteristics in a logic circuit and the gain of MOSFETs is revealed, the measurement of voltage and channel-length dependence of gain will be described. Finally, size limitation depending on the thickness of gate oxide will be discussed based on the relation between gain and channel length.

2. Gain of a MOSFET

The circuit diagram of a CMOS inverter is shown in Fig. 1. Here, logic threshold is assumed to be a half of supply voltage in order to maximize a noise margin. Under this constraint, the gain of an inverter is given as $(G_{\rm mp}+G_{\rm mn})/(G_{\rm dsp}+G_{\rm dsn})$, where $G_{\rm mp}$ and $G_{\rm mn}$ are transconductances of a P- and an NMOSFET, and $G_{\rm dsp}$ and $G_{\rm dsn}$ are drain conductances of a P- and an NMOSFET respectively. It is noted that the inverter gain is between the gains of a P- and an NMOSFET which are given as $G_{\rm mp}/G_{\rm dsp}$ and $G_{\rm mn}/G_{\rm dsn}$ respectively. The gain is measured where both $V_{\rm ds}$ and $V_{\rm gs}$ are a half of the supply voltage. As shown in Fig. 2, drain currents are measured with the gate bias voltage of $V_{\rm ds}+\Delta V$ and $V_{\rm ds}-\Delta V$ at ΔV intervals. The drain currents are differentiated to calculate the gain. Bias-voltage dependences of gain are measured at the channel lengths of 0.6 to 1.0 μm as shown in Fig. 3. Here, supply voltage corresponds twice as much as the bias voltage in Fig. 3 when the logic threshold of an inverter circuit is assumed. It is found that gain decreases as the channel length decreases and that there exists a maximum point of gain. The channel-length dependences of gain is shown in Fig. 4 at the biases of 1, 1.5 and 2 volts corresponding to the supply voltages of 2, 3 and 4 volts. It is found that the gain is nearly proportional to the effective channel length.

3. Origin of Gain Degradation in Short Channel MOSFETs

Drain current of a MOSFET changes by the modulation of channel potential, which changes by applying gate voltage through a gate insulator. When carriers in a channel region is assumed to travel at a saturation velocity $v_{\rm sat}$ due to the high internal electric field in a short-channel MOSFET, drain current $I_{\rm ds}$ is proportional to the the area density of charge Q and is given as $I_{\rm d}=W_{\rm g}v_{\rm sat}Q$, where $W_{\rm g}$ is gate width. Schematic capacitance network in a MOSFET is shown in Fig. 5, where Q changes by not only gate voltage but also drain voltage through drain capacitance $C_{\rm d}$. Consequently, the gain is nearly proportional to $C_{\rm g}/C_{\rm d}$. When the capacitances are approximated by one-dimensional model, gain G is given as

$$G=\frac{C_{\rm g}}{C_{\rm d}}=\frac{\epsilon_{\rm ox}}{T_{\rm ox}}\cdot\frac{L_{\rm g}}{\epsilon_{\rm Si}}=\frac{\epsilon_{\rm ox}}{\epsilon_{Si}}\cdot\frac{L_{\rm g}}{T_{\rm ox}}, \qquad (1)$$

where $T_{\rm ox}$ is the thickness of gate oxide, $L_{\rm g}$ is channel length, $\epsilon_{\rm Si}$ and $\epsilon_{\rm ox}$ are permittivities of silicon and gate oxide respectively. By substituting $T_{\rm ox}=11$ nm, $\epsilon_{\rm Si}=11.9$ and $\epsilon_{\rm ox}=3.9$, gain is calculated as 30 per one micrometer, which agrees with the measurement in the case of PMOSFETs in Fig. 4. The gain of NMOSFETs, however, is almost twice as large as the calculation although the gain is still nearly proportional to the channel length. The main reason is that the assumption of carrier traveling at a saturation velocity does not apply well to the NMOSFET case.

Although the gain may be improved through the suppression of electric field, it becomes more difficult to do this for sub-0.1-μm MOSFETs because the supply voltage are not scaled down proportionally to the channel length in order not to be affected by the fluctuation of threshold voltage. When the approximation (1) applies due to a high internal electric field in a sub-0.1-μm MOSFET, the gain as a function of channel lengths with parameters of several oxide thickness is shown in Fig. 6. If the lower limitation of oxide thickness is assumed 1.5 nm[3], the minimum channel length will be about 20 nm in order to obtain the gain of 5. For the further reduction of channel lengths, electric field suppression using drain and gate engineering will be required.

4. Summary

The relation between the gain of a MOSFET and a CMOS inverter was studied theoretically and experimentally. The voltage dependences of the gain in several kinds of MOSFETs were measured, where the gain is nearly proportional to channel length in the both cases of an NMOSFET and a PMOSFET. Origin of channel length dependence was discussed using a simple one dimensional capacitance model. For a sub-0.1-μm MOSFET, reduction of the internal electric field becomes more important not only to suppress the leakage current due to short channel effects but also to improve the voltage gain which is essential to active devices.

Acknowledgments

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References

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3) H. Momose, *et al.*:*Extended Abstracts of The Jpn. Society of Appl. Phys. and Related Societies* (1995) p. 751

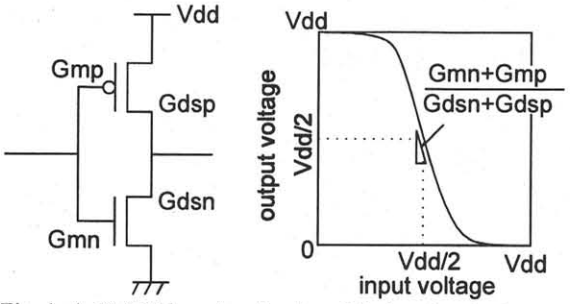

Fig. 1. A CMOS inverter circuit and its input-output characteristics. In the figure, Gmp and Gmn are transconductances of a P- and an NMOSFET and Gdsp and Gdsn are drain conductances of a P- and an NMOSFET respectively. Vdd is supply voltage.

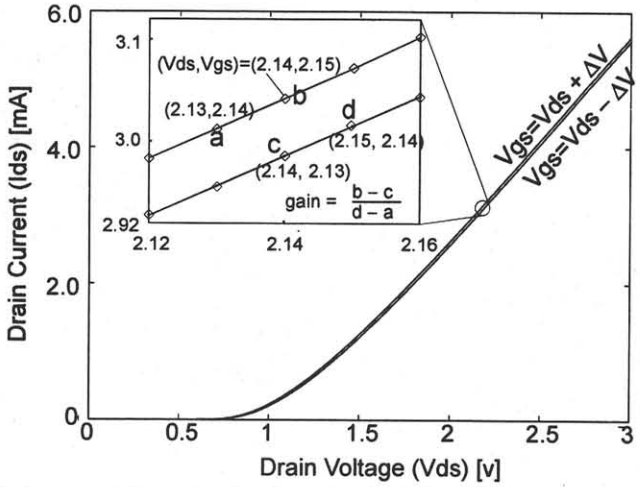

Fig. 2. A typical measurment of drain current characteristics for gain calculation. The gate voltage Vgs is set slightly higher or lower than drain voltage Vds in order to differentiate Ids. Imposed figure shows measurement points using gain calculation. In the figure, gain is calculated by dividing the difference of vertical points (b and c) by that of horizontal currents (a and d)

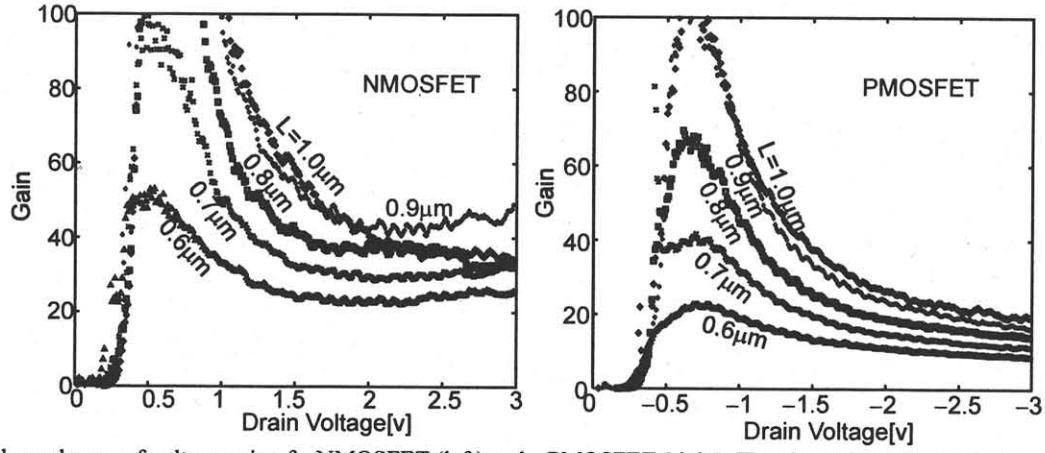

Fig. 3. Bias dependences of voltage gain of a NMOSFET (left) and a PMOSFET (right). The channel lengths are between 0.6 to 1.0 μm and gate oxide thickness is 11 nm. Both drain voltage and gate voltage are assumed equal to a half of supply voltage which maximize a noise margin of a logic circuit. The gain improves as a drain voltage decreases when it is more than 0.5 volt because the effective channel length increases and internal electric field is relieved.

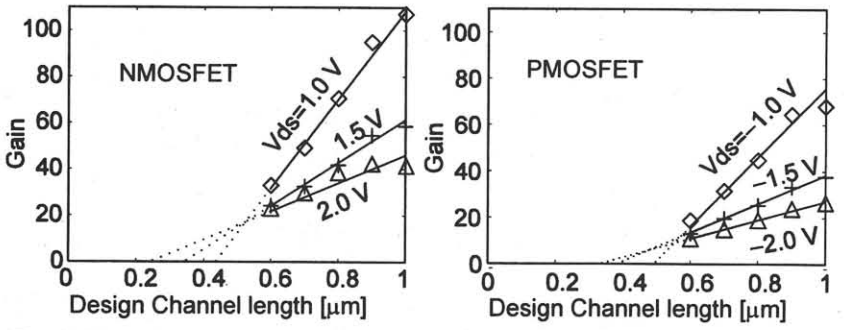

Fig. 4. Channel length dependence of the gains of a P- and an NMOSFET. The biases of 1.0, 1.5 and 2.0 volts in the measurement correspond to the supply voltages of 2.0, 3.0 and 4.0 volts in a logic circuit. The gain have nearly linear relation to channel length.

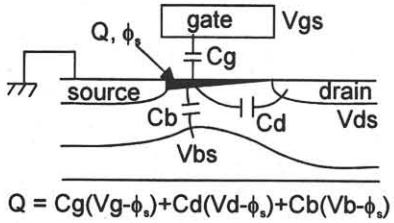

Fig. 5. Schematic capacitance network in a MOSFET. Cg, Cd and Cb are effective capacitances of gate, drain and substrate respectively. Q is area density of carriers and ϕ_s is the inversion potential.

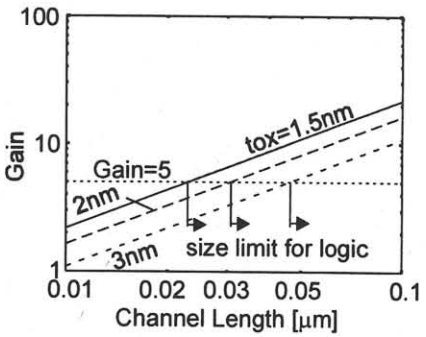

Fig. 6. Calculation results of channel length dependence of gain under the condition that the internal electric field is high enough for carriers to travel at saturation velocity.