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Photoresist CMP for Shallow Trench Isolation

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1. Introduction

Shallow Trench Isolation (STI) is one of the most important technologies for subquarter micron CMOS generation and beyond. Chemical Mechanical Polishing (CMP) is generally used as the planarization method for STI. To obtain excellent surface planarity by using CMP, various additional processes using a dummy pattern or polish stopper[1][2][3] have been proposed. These processes, however, increase the number of such process as exposure, deposition, and etching.

We developed a novel planarization method using photoresist(P.R.) as the CMP dummy pattern and polish stopper.

In this work, we investigated the CMP characteristics of P.R. and found that the P.R. polishing rates largely depend on the baking temperature. Using P.R. as a dummy pattern, we have devised a simple STI planarization process (by adding only two steps).

2. Experimental Procedures

First we investigated the relationship between baking temperature and P.R. polishing rates. For our experiments, we used commercially available posi-type P.R. of which the main solid sources are cresol-novolak and diazo-nophthoquino ne. P.R. was spin-coated on Si substrates, then baked for 20 min. on a hot-plate at 100℃. P.R. thickness was about 2 μ m. Then we baked the wafers for 20 min. on a hot-plate at temperatures raging from 120℃ to 260℃. We measured the polishing rates, hardness and FT-IR spectra for each sample.

In this study, we used a dead-weight type of polishing machine and commercially available colloidal silica slurry. Table 1 lists typical P.R. polish conditions.

3. Results and Discussion

P.R.CMP

Figure 1 shows the dependence of P.R. polishing rates on baking temperature. The P.R. polishing rates were drastically reduced with increasing baking temperature. The P.R. polishing rate exceeded 7000nm/min. after baking at 170℃, but matched the value (80nm/min.) of SiO_2 after baking at 220℃. The polishing rate ratio ($PR_{170℃}/PR_{220℃}$) is 87.

Figure 2 shows the variation in P.R. hardness according to baking temperature. The P.R. hardness gradually increases with higher baking temperature. The P.R. hardness after baking at 260℃ is about 0.75 GPa, which is only 1/15 of the hardness of fused silica (11 GPa).

Figure 3 plots of the P.R. polishing rates versus P.R. hardness. The P.R. polishing rates are logarithmically dependent on P.R. hardness. Accordingly, the P.R. polishing rates can be controlled in a wide range of baking temperature. P.R. baked at the same polishing rate as SiO_2 is appliciable to the dummy pattern, and baking at a polishing rate less than that of SiO_2 is suitable for the polish stopper for CMP.

Figure 4 shows the dependence of FT-IR spectra on baking temperature. Notable differences are seen in four wavenumber regions. Table 2 summarizes these wavenumber regions. At a baking temperature of 120℃, two peaks (1500cm^{-1}, 1600cm^{-1}) originating from Benzene rings are observed. These peaks are weakened with increased baking temperature. This means that Benzene rings have dissolved. The other two peaks (3000-2300cm^{-1}, 3500-3300cm^{-1}) originate from the $N\text{-}H^+$ and O-H, N-H bonds. These two peaks change into a single broad peak as baking temperature increases. This means that $N\text{-}H^+$ becomes N-H, and that oxyhydride is desorbed. We consider the changes in P.R. polishing rates to be caused by a transition in P.R. composition.

STI process

The STI planarization process using dummy pattern[1] requires exposure, planarizing resist coating and the etch-back process. Uniformity and strict control are essential for the etching process because both strongly affect the final uniformity of field oxide thickness. We can reduce the number of etching steps by using P.R. CMP. Figure 5 shows the proposed process flow.

1)After trench etching, AP-CVD SiO_2 was deposited to refill the trenches.

2) P.R. was patterned on the field region using photolithography and baked to adjust the polishing rates between P.R. and CVD SiO_2.

3)Planarize P.R. and CVD SiO_2 at the same time using CMP.

Figure 6 shows a cross-sectional SEM image during CMP. P.R. and SiO_2 are polished at the same polishing rate, then P.R. serves as an effective dummy. There is no problem regarding the adhesiveness between P.R. and SiO_2.

4. Conclusion

We developed a novel STI planarization process using P.R. as a CMP dummy pattern. We found that P.R. polishing rates are logarithmically dependent on baking temperature. The polishing rate ratio ($PR_{170℃}/PR_{220℃}$) is 87. By using P.R. CMP, we were able to devise a simple STI planarization process.

Acknowledgements

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References

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[2]K.Blumenstock et al. J. Vac. Sci. Technol. B21(1), Jan./Feb. (1994) 54
[3]B.H Roh et al. SSDM Ext. Abs. (1995) 590

Table 1 Typical P.R. polish conditions.

Pressure (g/cm^2)	230
Head rotating speed (rpm)	60
Table rotating speed (rpm)	60
Slurry flow (cm^3/min)	100

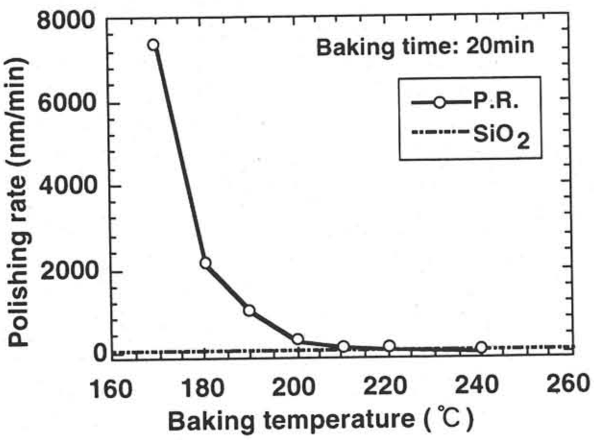

Figure 1 P.R. polishing rates versus baking temperature.

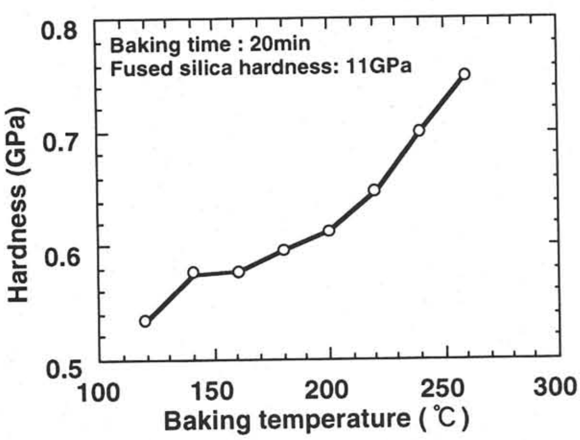

Figure 2 P.R. hardness versus baking temperature.

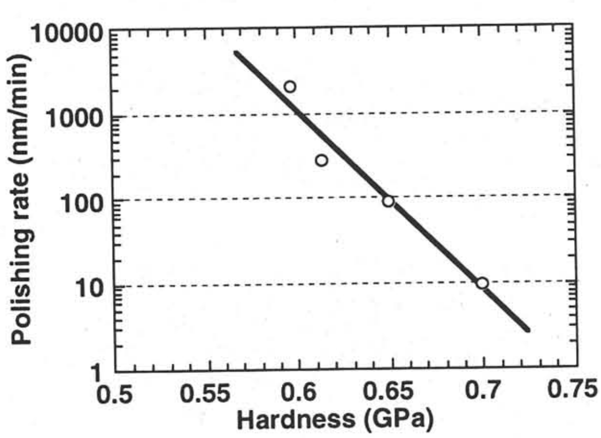

Figure 3 P.R. polishing rate dependence on P.R. hardness.

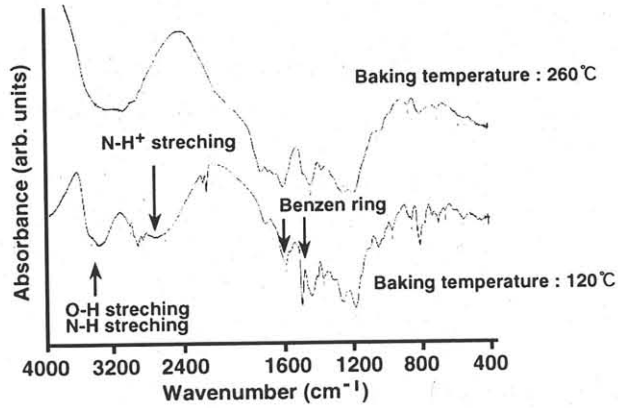

Figure 4 FT-IR spectra after baking.

Table 2 Typical wavenumber regions.

Wavenumber (cm^{-1})	Origin	120℃	260℃
1500	Benzen ring	◎	△
1600	Benzen, N-H	◎	△
3000-2300	$N\text{-}H^+$	○	Become one broad peak
3500-3300	O-H, N-H	○	

◎ Very strong
○ Strong
△ Weak

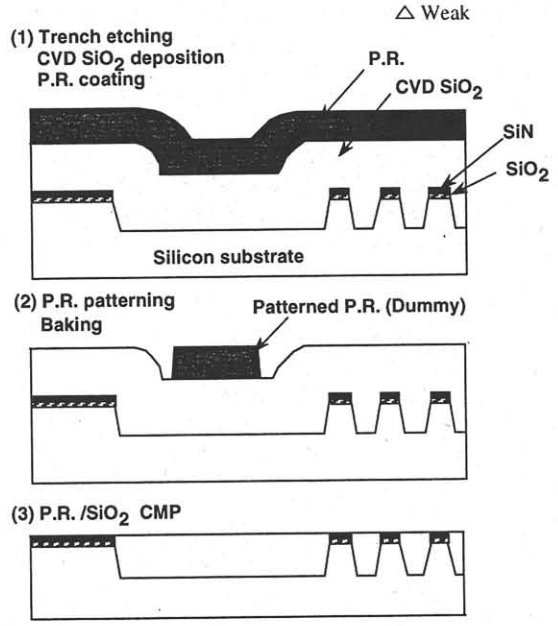

Figure 5 STI process flow using P.R. CMP.

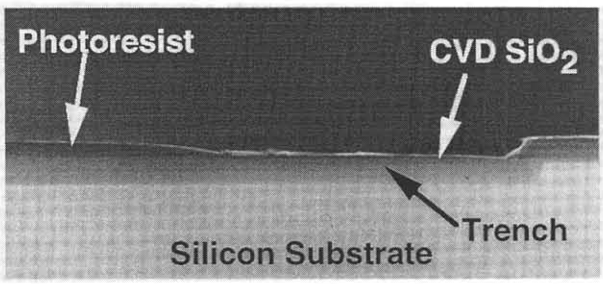

Fig.6 Cross-sectional SEM image during P.R./SiO_2 CMP.