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Optimization of Process Conditions for Quarter Micron Recessed Poly-Si Spacer LOCOS (RPSL) Isolation

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1. Abstract

Direct application of the RPSL isolation to the quarter micron devices generates unacceptably high stress at the edge of the isolation region due to the suppression of the bird's beak encroachment. Here, we propose two optimization methods of the RPSL isolation for those devices. Both of the conditions have increased TDDB characteristics and the improvements are also proved from the lowered edge failure ratio on gate patterns.

2. Introduction

As a device dimension has been scaled down, the bird's beak encroachment became one of the most serious problems in LOCOS type isolation. To reduce the bird's beak encroachment, we must use a thick SiN and a thin pad oxide on the active region. However, this process condition generates steep profile in an isolation edge and so a concentration of a stress. This stress concentration at the isolation edges can lead to a high junction leakage current and degradation of the gate oxide reliability [1, 2]. In this paper, we show that the major factor of the degradation is the mechanical stress which is induced during the RPSL process [3], and suggest methods of eliminating the gate oxide degradation by reducing the mechanical stress.

3. Experiments

Fig. 1 represents process steps of the RPSL. At first, 1st pad oxide and a SiN layer were deposited and etched for a field area opening. Then, the exposed substrate Si was etched slightly (Fig. 1 (a)). An isotropic etch of the pad oxide was followed and poly-Si spacers were formed beside the SiN (Fig. 1 (b)). Then, a field oxidation step was performed (Fig. 1 (c)). SiN was removed, a sacrificial oxidation, etching of it, another oxidation as a buffer layer for the ion implantation, and its removal make the final isolation profile as shown in Fig. 1 (d).

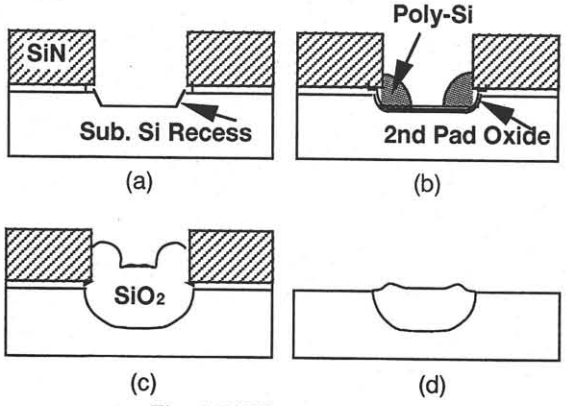


Fig. 1 RPSL process steps.

Critical parameters for the gate oxide degradation are thicknesses of the active SiN and the 2nd pad oxide. Therefore, we made the active SiN with the thicknesses of 150, and 200 nm, and the 2nd pad oxide with the thicknesses of 4, 5, and 6 nm, respectively. Stress releasing schematics are organized with adding an annealing step after the sacrificial oxidation [4], and with making a CVD 2nd pad oxide [5, 6].

4. Results and Discussion

Fig. 2 shows TDDB characteristics. Combinations of 200 nm / 4 nm and 200 nm / 5 nm (active SiN / 2nd pad oxide) show low TDDB characteristics than other combinations. Fig. 3 shows junction leakage currents with the same combinations and identical as the TDDB. It means that the stress with a combination of a thick SiN and a thin 2nd pad oxide is larger than with the opposite combination.

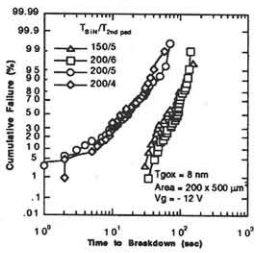


Fig. 2 TDDB data with various process conditions.

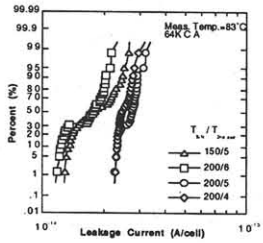


Fig. 3 Cell junction leakage current data with various process conditions.

However, that is inevitable for the active opening of a quater micron device. The SEM profiles in Fig. 4 represent a steep active/field boundary and a thinning of the gate oxide on a boundary with the combinations of 200 nm / 4 or 5 nm.

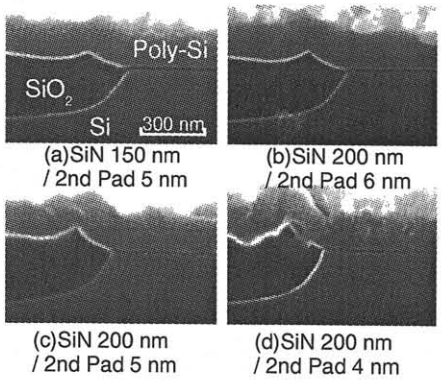
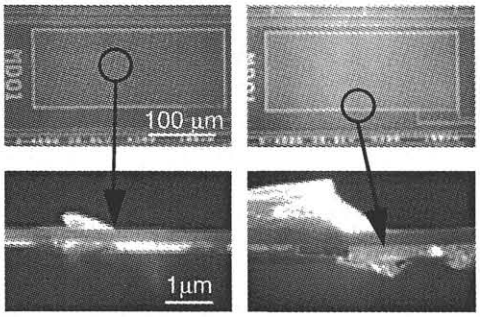


Fig. 4 Final isolation profiles with various process conditions and gate oxide thinning in each case.

It is thought that if a breakdown occurs at the center of a test pattern, the breadown originates from an intrinsic degradation (Fig. 5 (a)), but if it occurs at an edge, the breakdown depends on an isolation edge condition (Fig. 5 (b)). Fig. 6 shows a relation between the breakdown position and TDDB time. As the edge breakdown percentage goes higher, the time to breakdown goes shorter, and this explains a reason of the shorter TDDB time in 200 nm / 4 or 5 nm cases. We can interpret that isolation edges get weakened by the process of suppressing the bird's beak encroachment.



(a) (b)

Fig. 5 SEM micrographs of the gate oxide breakdown. (a) Center Breakdown. (b) Edge Breakdown.

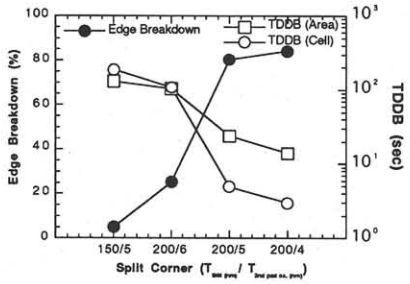
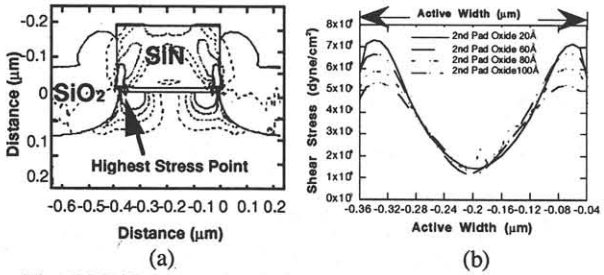


Fig. 6 Relation of the breakdown position with TDDB time.

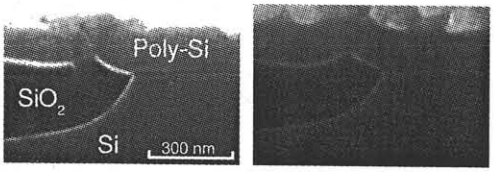
Fig. 7 (a) is a simulation result of RPSL process by TSUPREM-IV. It shows that a stress concentrates at field oxide edges. Fig. 7 (b) shows stresses along with a horizontal active region and shows that higher stress concentration is observed with the thinner 2nd pad oxide.



(a) (b)

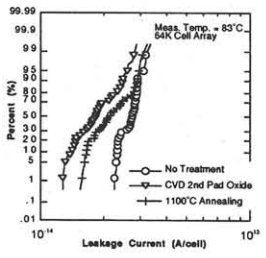
Fig. 7 RPSL stress simulation results in (a) 2-D and (b) 1-D. TSUPREM-IV was used.

Fig.8 shows profiles of adding an annealing step after the sacrificial oxidation (Fig. 8 (a)) and substituting the thermally grown 2nd pad oxide for the CVD 2nd pad oxide. Each of them shows almost the same profile as Fig. 4 (c). However, their cell junction leakage currents (Fig. 9) and the TDDB times (Fig.10) show much improved characteristics. In addition, the edge breakdown percent became lowered as well. It is considered that the stress relieving by adding an annealing step or the lowered stress by substituting for the CVD 2nd pad oxide enhances the gate oxide growth at edges while guaranteeing a fine active opening for the quater micron devices.



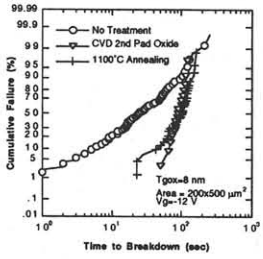
(a) (b)

Fig.8 SEM micrographs of the stress released RPSL isolation. (a) 1100°C annealing and (b) 5 nm CVD 2nd pad oxide.



(a)

Fig. 9 Cell junction leakage current data with the stress released RPSL isolation.



(b)

Fig. 10 TDDB data of the stress released RPSL isolation.

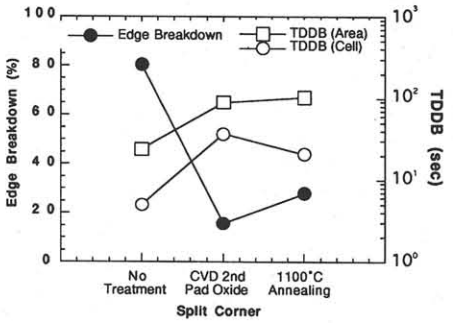


Fig. 11 Edge breakdown vs. TDDB time in the stress released RPSL isolations.

5. Conclusion

Through a series of experiments, we showed that a degradation of the gate oxide reliability with RPSL is due to the stress concentration at the active/field boundaries and proposed two methods of relieving it. These are adding a high temperature annealing step and depositing a CVD 2nd pad oxide instead of thermally grown one, and using these techniques, we could improve the gate oxide reliability.

References

1. H. Uchida et. al., *IEEE Trans. on Elec. Dev.*, Vol. ED-40, No. 10, p. 1818, 1993.
2. P. Smeys et. al., *IEDM Tech. Dig.*, p. 709, 1996.
3. D. H. Ahn et. al., *IEDM Tech. Dig.*, p. 679, 1994.
4. S. Wolf., "*Silicon Processing for the VLSI Era*", *Vol.* 3, p. 459, 1995.
5. I. Magdo et. al., *J. Electrochem. Soc. Vol. 125*, p. 932, 1987.
6. J. C. Lee et. al., *IEEE Trans. on Elec. Dev.*, Vol. ED-38, No. 12, p. 2268, 1988.