Effects of Buffer Layer Structure in Poly Buffered LOCOS for Deep Submicron Silicon Devices

Jong-Ho Lee, Tae Moon Roh, Jong-Son Lyu, Bo Woo Kim, and Hyung Joon Yoo
1Semiconductor Technology Division, ETRI, Taejon 305-600, Korea
2School of Electrical Eng. Wonkwang University, Iksan, Chonpuk 570-742, Korea
Phone/Fax: +82-653-50-6695, E-mail: jhlee@wonms.wonkwang.ac.kr

1. Introduction
As silicon device size scales down, conventional LOCOS becomes insufficient for the isolation of deep submicron devices. Of more advanced isolation technologies to substitute the conventional one, Polysilicon Buffer LOCOS (PBL) is very promising method due to its simplicity and less bird’s beak encroachment into active region [1]. However, problems of conventional PBL are its lack of smooth edge morphology [2] and microtrenchings [3]. Recently, a new approach based on in-situ nitrogen doped buffer layer was proposed to suppress the grain growth of the buffer layer during heat cycle [4] and solved the problems.

In this paper, we introduce a new method to suppress the grain growth of the buffer by adopting multi-layered buffer structure, which is the simplest of advanced PBL technologies. Effects resulted from the structure of the buffer layer are reported.

2. Sample fabrication
The process steps for sample fabrication are shown in Fig. 1. The only difference from conventional PBL is the multi-layered structure of the buffer layer as shown in split condition of Table 1. The pad oxide was grown to a thickness of 10.8 nm and followed by the formation of undoped buffer layer by LPCVD. The total thickness of the buffer layer is 60 nm and details are illustrated in Table 1. Buffer layer of sample p1 is polysilicon deposited at 625 °C and those of other samples are amorphous silicon (a-Si) deposited at 550 °C. The multi-layer structures are formed by adopting a-Si, since thin film formation by using a-Si is easier than polysilicon. Multi-layered structure in a buffer layer was formed by repeating atmospheric pressure/LPCVD without breaking the process step. Subsequently Si3N4 was deposited by LPCVD to 150 nm. Active regions were masked by photoresist and then Si3N4/buffer layers are vertically etched away by anisotropic RIE. A 390 nm thick field oxide was grown at 925 °C in steam ambient. Nitride layer for the active region was stripped in conventional wet solution. Parts of wafers were processed to obtain the effect of buffer structure on electrical characteristics of conventional NMOS devices.

3. Effects of the buffer structure in PBL
Fig. 2 shows the 45° tilted SEM views of 4 samples after removing the buffer layer by anisotropic RIE (10 % overetch). Sample p1 shows rough edge morphology and randomly distributed microtrenchings. The rough edge morphology is attributed to the well known random orientations of polysilicon, grain size, and oxidation rate at grain boundary.

In sample a1, we can observe the line-type microtrenching and rough surface of active region resulted from the recrystallization of a-Si to larger grain size. Sample a2 shows randomly located point-type microtrenchings but relatively smoother edge morphology than that of sample p1. Sample a3 only shows no microtrenchings and the smoothest edge morphology. Fig. 3 shows the TEM photographs for samples p1 and a3. Multi-layered structure of sample a3 is clearly shown and smaller grain size than that of sample p1 is observed. We can find the rough morphology under the buffer layer in bird’s beak region of sample p1 while not in sample a3. The oxygen depth profile obtained by SIMS analysis is shown in (b). We can observe oxygen peaks at each vertical grain boundary, which exactly correspond to the TEM result. The oxygen peaks between a-Si layers gives a possibility of very thin (nearly native) oxide growth during each atmospheric pressure (AP) period of repeated AP/LPCVD modes in a furnace at 550 °C. To obtain electrical data, we fabricated NMOS devices with 4 different PBL LOCOS process. Fig. 4 shows gate oxide breakdown voltage distributions measured from 98 devices of each sample. Average breakdown voltages for all samples are reasonable (larger than 9.3 V, ∼1.5 MV/cm). However, we can observe the significant difference of distributions of breakdown voltages. Sample p1 shows no distinct peak of bin. As the number of a-Si layer at fixed buffer thickness increases, we can obtain better distribution and higher average breakdown voltage. The results mean the gate oxide thinning effect can be improved by the multiple buffer structure.

4. Conclusions
We reported the effect according to the buffer layer structure in PBL. By increasing the number of buffer layer while keeping total thickness the same, we obtained smooth edge morphology, no microtrenchings, and better gate oxide breakdown distribution.

References
Fig. 1. Schematic process steps for PBL isolation.

Fig. 2. 45°-tilted SEM microphotographs after the dry etching of the buffer layer. Rough edge and point-type microtrenching is observed in sample p1 as shown in figure (a). Figure (d) shows no microtrenching and smooth edge.

Fig. 3. TEM cross-sectional views of typical PBL (poly-Si: p1) and new MPBL (a-Si/a-Si/a-Si: a3). Triple-layered structure of the buffer layer (sample a3) is clearly shown in figure (b). The grain size in (b) is smaller due to the structure.

Fig. 4. Measured gate oxide breakdown voltage distributions of samples p1 (a), a1 (b), a2 (c), and a3 (d). Sample p1 shows no distinct peak of distribution. Sample a3 shows the best characteristics.