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Shallow Trench Isolation Characteristics with High-Density-Plasma (HDP) CVD Gap-Fill Oxide for Deep-Submicron CMOS Technologies

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1. Introduction

As design rules of CMOS technologies are scaled down to deep submicron technologies for giga bit DRAM era, Shallow Trench Isolation (STI) becomes the very effective way to meet tight design rules and also high performance device requirements. Gap-filling of very narrow trench spaces and trench top-corner profiles are the most critical issues in developing STI technologies to date. Recently, HDP CVD oxide has been shown for the viable filling capability of very narrow gap and superior isolation characteristics as well as the advantages of low HF etch rate and good planarity due to non-conformal bottom-up coatings [1-3]. This paper systematically studies STI characteristics based on void-free gap-filling conditions of inductively coupled (ICP) HDP oxide with various Deposition/ Sputtering (D/S) ratios along with different trench sidewall (S/W) oxide thicknesses. Splited deposition conditions, i.e. ① D/S=3.2, ② 5.1+3.2, ③ 8.0+5.1+3.2, are used to evaluate the sputtering effects on Si-surface, causing diode edge intensive leakage current. Each split condition is carried out by thin high D/S followed by thick low D/S HDP all in *in-situ* manner. With these ratios, trench sidewall thermal oxides are also varied to cure Si-etch damages, round trench top corners, and protect trench surfaces from the sputter effect of HDP. Measurement results include diode leakage current, narrow width effect, subthreshold characteristics, latchup, GOI, and isolation punchthrough voltages with an optimized CMP and HF wet cleaning processes.

2. Experimental

Sample devices are fabricated on (100) oriented p-type Si-wafers with resistivity of 9-12 Ω-cm. The key STI process sequences start with pad layer formation, followed by active pattern definition. Trench etch is then processed to form tapered angle of ~83° and depth of 0.3μm. Thermal oxides of 0Å~200Å are grown on the trench surfaces in 5% DCE (DiChloroEthylene) ambient at 900°C to cure the etch damage and round trench top corners. Total HDP oxide thickness of 7500Å is deposited at 350°C to fill narrow trenches. Each splits are performed for *in-situ* HDP deposition of ① 7500Å, ② 1500Å followed by 6000Å, and ③ 1000Å+1000Å+5500Å in sequence. After CMP planarization, the oxides are densified at 1000°C for 30 min. in N_2 ambient to lower the HF etch rate whose etch rate are summarized in Table I. The retrograde twin well implants and channel stop (CS) implants are then processed, and followed by pad-oxide removal, sacrificial oxidation, channel Vt adjust implants, and gate oxide growth after removal of the sacrificial oxide. The final trench profile with tapered angle and rounded corner is shown in Fig. 1.

3. Results and Discussion

The Fig. 1 (a) & (b) show the final STI profile with good planarity and rounded corners for S/W oxide of 68Å and hump-free subthreshold I_D-V_G for Vsub=0V and -3V. The trench top corner is not rounded for no S/W oxide (not shown) which resulted in random hump characteristics due to field crowding effect at sharp corners.

Table I: HF etch rate of HDP vs. thermal oxide

D/S ratio's		3.2	3.9	5.1	8.0	Therm. ox
HF etch rate vs. thermal ox	As-dep	2.02	2.20	2.43	2.69	1.00
	Anneal (1000C)	1.25	1.27	1.23	1.24	1.00

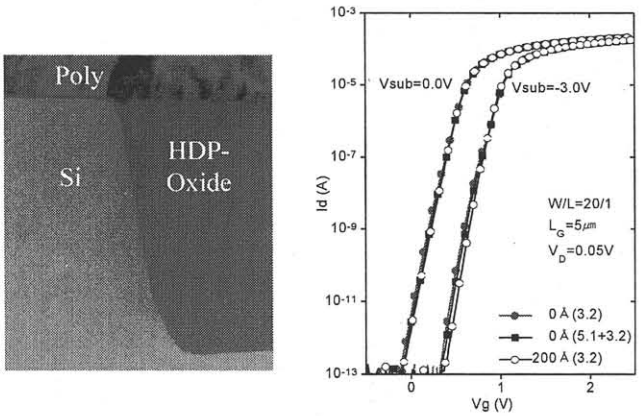

Fig.1 (a) TEM picture of finished STI profile with S/W oxide of 68Å and (b) subthreshold I_D-V_G characteristics

Fig. 2 shows threshold voltage shift, $\triangle V_T$, vs. gate width. The fixed charge density at the interface of the trench and boron segregation into S/W oxide can enhance the edge conduction or lower the edge V_T of nMOS more than of pMOS with the reduction of the channel width, resulting

INWE and NWE, respectively [4]. Process optimizations to suppress the trench corner effect are done for ΔV_T between W=0.3μm and 5μm to be less than 130mV for nMOS and almost no NWE for pMOS, which is the lowest value reported with HDP [1-2]. Note that NWE's of no S/W oxide and high D/S samples are slightly degraded probably due to sharp edge corners. Fig.3 shows that the isolation breakdown

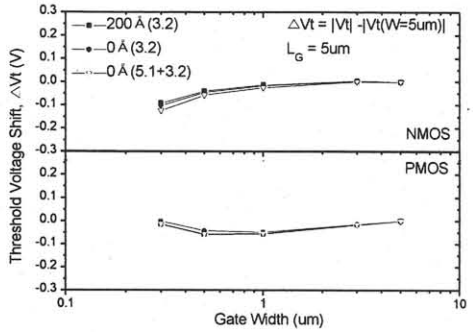

Fig. 2 The threshold voltage shifts, $\triangle V_T$, between W and W=5μm for both nMOS with INWE and pMOS with NWE.

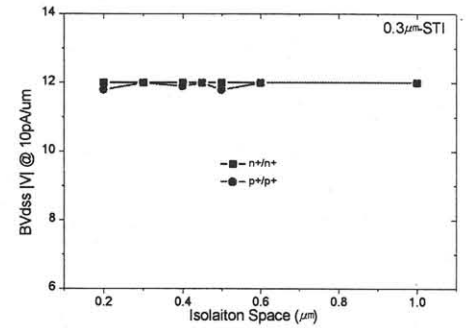

Fig. 3 The n+/n+ or p+/p+ isolation punch-through voltage characteristics

voltages (BVdss) higher than 11V are obtained down to the minimum space of 0.2μm, which is insensitive to S/W oxide thickness, D/S ratio, and CS implant. Fig. 4 shows the latchup holding voltage, V_H, vs. n+/p+ spacing, channel stop implant, compared to LOCOS. The measurement indicates the improvement of V_H for STI and CS implant case simply due to effectively thicker field oxide and less well resistance R_W, respectively. Fig. 5 compares sputter effect of HDP or Si-etch damage on trench surface through diode leakage current. The leakage data shows that the HDP stress induced leakage current and sputtering effects are negligible in our ICP HDP system. However, the leakage is slightly larger for S/W oxide of 200Å than 0Å. This implies that there is no apparent etch damage, but thick S/W oxidation can introduce the stress induced leakage. Moreover, the leakage can also be introduced from the weak trench corners due to the larger plasma etch during FG sidewall formation after CMP processes when they are exposed for successive HF cleanings in weak active edges. This phenomena can also be seen in gate oxide charge-to-breakdown data shown in Fig. 6, which results in slightly worse GOI characteristics in field-butted pattern than non-field butted pattern.

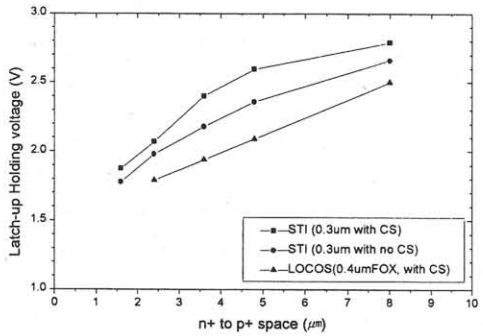

Fig. 4 The latchup holding voltage vs. n+/p+ spacing

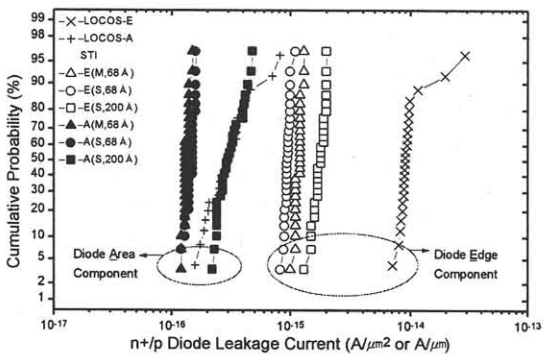

Fig. 5 n+/p diode leakage current with split conditions at V_R=4.0V, compared to LOCOS(1900Å/100Å: Nit/oxide): E (Edge), A(Area), S (Single D/S , 3.2), M(Multi D/S, 8.0 + 5.1+3.2)

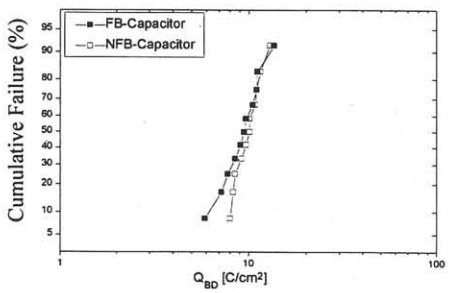

Fig. 6 The Gate oxide charge-to-breakdown at J=-100mA/cm^2 between field butted and non field butted capacitor pattern.

4. Conclusion

The HDP gap-fill material with sidewall oxide is extensively characterized to study STI characteristics. The leakage data shows the sputtering effect on trench sidewall is negligible even for the high sputter condition (low D/S) in our system and the Si etch damage is very small so that the leakage is almost independent of S/W oxide thickness, but becomes appearing stress induced leakage for thick oxide (> 200Å). The trench edge conduction is, however, mainly enhanced from the weak trench corners due to post CMP processes when they are exposed for successive HF cleanings in weak active edges.

References

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