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# A Characteristics of Buried Channel Poly-Si TFTs

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## 1. Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) at low temperature have attracted much attention in various large area electronic applications such as flat panel displays, page width optical scanners and page width printer heads. In conventional poly-Si TFT, the drain has to be offsetted from the channel region in order to achieve low leakage current. However, this causes severe current pinching problem, resulting in high on-resistance. Recently, a field plated high voltage TFT was proposed to solve the problem. It offers higher current driving capability without increase the leakage current[1]. However, this approach results in a complicated device structure and biasing scheme. In addition, the driving current level and switching speed are more important performance in case of poly-Si TFT LCD panel application. It is well known that the buried channel MOSFETs has higher mobility that that of surface channel devices[2]. The purpose of our work is employing the buried channel for increase the ON-current and obtaining the higher operating frequency.

## 2. Device Structure and Fabrication

In this paper, we propose a fabrication method for CMOS TFTs with buried channel(BC TFT). The proposed device has been fabricated by implantation doping of poly-Si active buried channel layer and we have designed four terminal electrodes TFTs rather three terminal conventional TFTs. Compared with the conventional poly-Si TFTs, the device has two unique things. The one is the buried channel of active layer for conductivity modulation and the other is the fourth terminal entitled back bias for preventing kink effect and malfunctioned driver for TFT LCD with driving circuit integration.

The schematic diagram of proposed buried channel TFT is shown in Fig. 1. The process sequences to form the buried channel is as follows in case of n-type poly-Si active buried channel layer doped by implantation. We employed 5000Å wet oxidized silicon wafer for emulating quartz substrate. The 500Å thick a-Si film was deposited by LPCVD system. $BF_2^+$ ions ($1\times10^{12}cm^{-2}$, 30KeV) are implanted in order to form p-type back channel conductivity modulation layer. The 500Å thick a-Si film was deposited and the 1000Å thick implantation sacrificial TEOS layer deposited and $As^+$ ions ($1\times10^{14}cm^{-2}$, 70KeV) are implanted into the buried channel forming region. The excimer laser recrystallization was performed. At this time, $BF_2^+$ ions diffused from lower implanted a-Si layer and $As^+$ ions was activated by laser energy so that doping profile for buried channel was obtained.

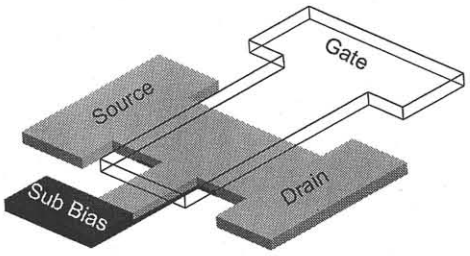


Fig. 1 The schematic diagram of proposed Buried channel TFT.

## 3. Experimental Results

Fig. 3 shows a SIMS profile of active layer doping concentration fabricated by proposed method. Fig. 2 shows the $I_D$-$V_G$ characteristics of the new and conventional poly-Si TFTs, of which the channel length and width are 2㎛ and 10㎛. The proposed device exhibits superior performance to conventional poly-Si TFTs in on-current(field effect mobility) and leakage current.

We fabricated the 23-stage CMOS inverter chain (ring oscillator) in order to make a comparison of dynamic characteristic between conventional poly-Si TFT circuit and proposed buried channel poly-Si TFT circuit. The size of nMOS and pMOS TFTs of CMOS ring oscillator have been optimized to W/L=10㎛/6㎛ and 20㎛/6㎛ respectively. The output frequency of the ring oscillator was measured by Tektronix 2430A digital oscilloscope, and plotted as a function of operation voltage($V_{DD}$) as shown in Fig. 5. The operating speed of ring oscillators with buried channel is much higher than that of ELA active film. This result is caused by effects of device ON-current, and mobility.

## 4. Conclusion

We have successfully investigated the characteristics of buried channel poly-Si TFT devices and circuits fabricated. It should be noted that the ion shower process may be applicable to fabricate the BC poly-Si TFT, although the impurity doping for forming buried channel was performed by ion implantation. In order to investigate the dynamic characteristics of the poly-Si TFTs processed with various methods, we have fabricated and measured the operation frequency of 23-stage CMOS ring oscillators. The ring

oscillators with BC poly-Si TFT operate at much higher speed (at lower $V_{DD}$) than that of conventional poly-Si TFT, due to effects of device ON-current and mobility.

## Reference


1) T.Y. Huang, I.-W. Wu, A.G. Lewis, A. Chiang, and R.H. Bruce, IEEE Electron Dev. Lett., **11** (1991), 541
2) M.J. Van der Tol and S. G. Chamberlain, IEEE Electron Dev., **40** (1993), 741


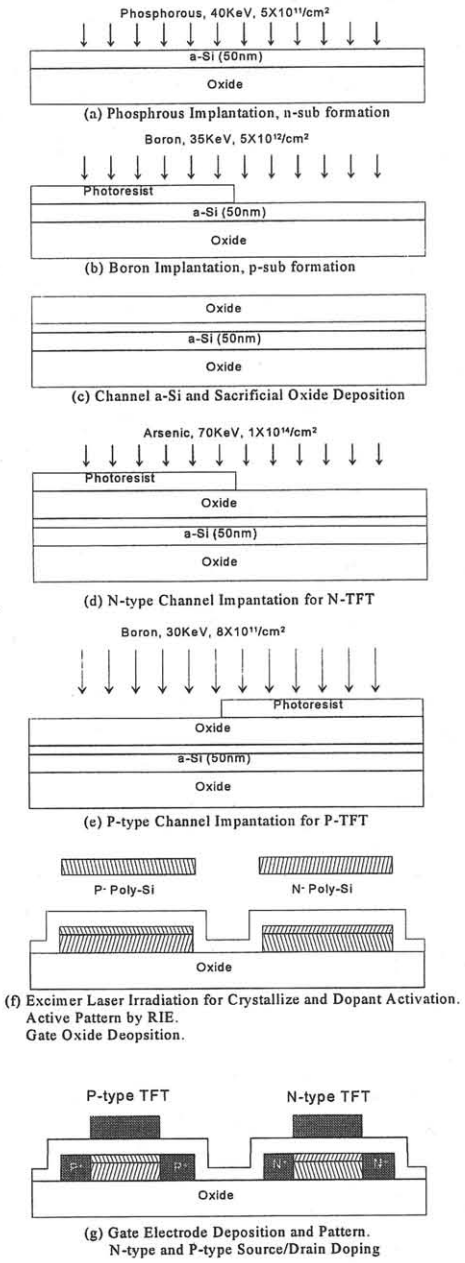


Fig. 2 Fabrication step of proposed BC TFT.

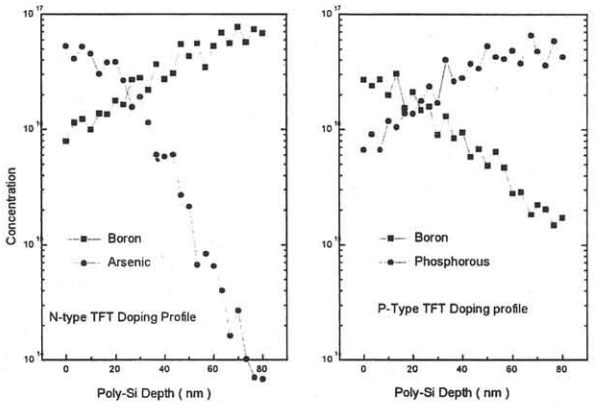


Fig. 3 SIMS profile of fabricated BC TFT active channel

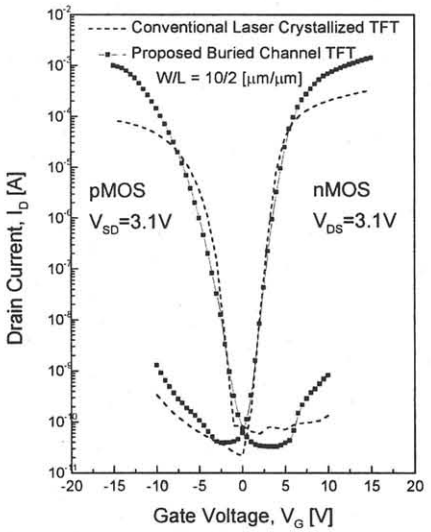


Fig. 4 Transfer characteristics of conventional and novel buried channel TFT.

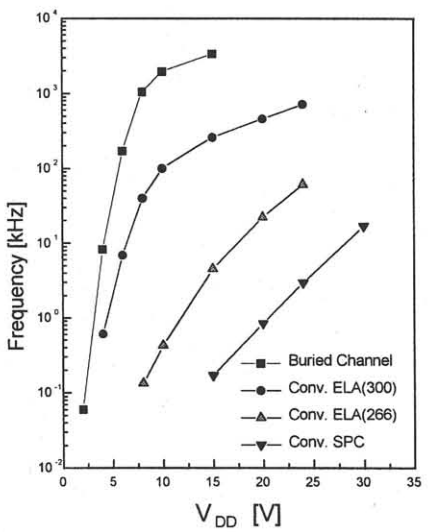


Fig. 5 The operation frequency of 23-stage CMOS ring oscillators as a function of $V_{DD}$.