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New Poly-Si Thin Film Transistors with a-Si Channel Region Designed to Reduce the Leakage Current

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1. Introduction

Poly-Si TFT's are promising devices for active matrix liquid crystal displays (AMLCD's) because of their high carrier mobility and driving current capability. The fabrication of pixel matrix and peripheral driving circuits on the low cost glass substrate with poly-Si TFT's may reduce manufacturing cost. However, it is well known that the leakage current in poly-Si TFTs due to defects in grain boundary causes a serious problem in pixel element[1]. LDD (lightly doped drain) structure or offset structure has been proposed to reduce the leakage current by reducing the electric field in the depletion region near the source/drain, while those structures result in decrease of ON-current because of a comparably high resistance of LDD or offset region[2].

Purpose of this paper is to propose the new poly-Si TFT which reduces the leakage current effectively without significant reduction of ON-current. We employ high resistive amorphous silicon region in the channel near the source/drain instead of LDD or offset region. In the fabrication of the proposed device, we eliminated an additional mask and mis-align problem by employing photoresistor reflow method maintaining self-alignment[3].

2. Device Structure

The schematic view of the proposed poly-Si TFT is shown in Fig. 1. The amorphous silicon region, which has very high resistance, is more effective in reducing the leakage current than LDD or offset region. In order to prevent the significant decrease of ON-current in our proposed device, a-Si region is located under the gate electrode and this is the main structural difference compared with conventional LDD or offset poly-Si TFT's.

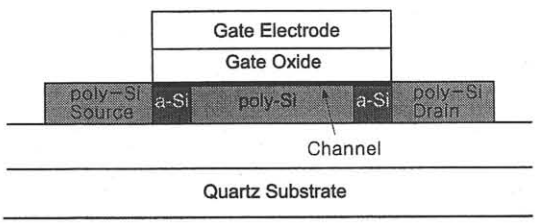

Fig 1. Schematic feature of the proposed poly-Si TFT structure

Under the ON state, the field induced electron carriers at the a-Si region forms the continuous path of ON-current with the main poly-Si channel. Therefore, ON-current does not decrease much because the channel is clearly formed between the source and drain. In order to fabricate the selectively crystallized active layer, we employ the excimer laser crystallization method and make the laser beam transmitted selectively onto the active layer with the help of the patterned metal.

3. Device Fabrication

The process sequences are as follows. 800 Å thick a-Si film is deposited by LPCVD on the quartz substrate and patterned for active island. 1000 Å thick TEOS gate oxide layer and 1000 Å thick ITO gate electrode are successively deposited. Next, the proposed selective crystallization method is carried out and it is shown in Fig. 2.

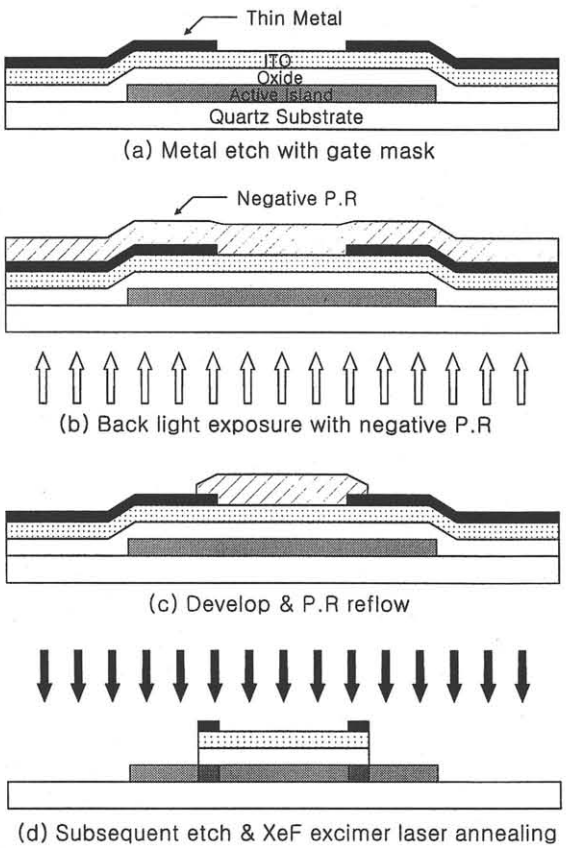

Fig. 2 Fabrication process for the proposed device

Thin aluminum metal layer is deposited on the ITO layer and patterned by photo lithography with negative photoresistor as shown in Fig 2 (a). Another photomasking step with the backlight exposure is carried out as shown in

Fig. 2 (b). We do not need any additional mask because the aluminum pattern on the ITO layer automatically acts as photo mask. The patterned photo resistor is reflowed at 160 ℃ for 20, 30 and 40 minutes as shown in Fig. 2 (c). We employed photo resistor reflow method to eliminate the mis-align problem. After subsequent etch of Al and ITO gate electrode, Al pattern surrounds the side of ITO gate. At this time, the XeF excimer laser crystallization is carried out at the energy density of 250mJ/cm^2. The XeF excimer laser is employed because it has long wave length (λ =351nm) which penetrates transparent ITO film without significant energy loss[4]. Consequently, we can obtain the selectively crystallized active layer as shown in Fig. 2 (d) because the laser beam can not penetrate the metal pattern. The length of amorphous region is the same as the width of the Al pattern. Finally, we finish the fabrication of the device after source/drain ion-shower doping, which does not need any post-annealing step, and metallization process for contact.

4. Experimental Results

Fig. 3 shows the transfer characteristics of the proposed and conventional poly-Si TFT's. The ON-current of proposed TFT with 0.5 ㎛ amorphous region has little difference compared with that of conventional one, while the leakage current is remarkably reduced due to the high resistive a-Si region in the channel.

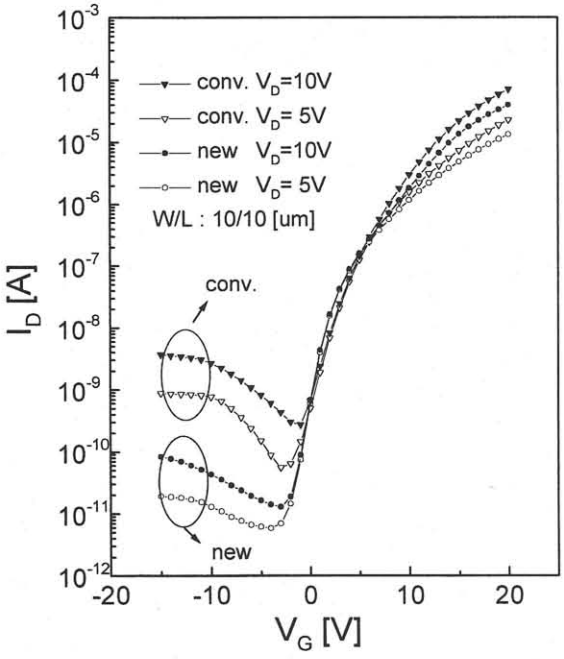

Fig. 3 The transfer characteristics of the proposed and conventional TFT's

The leakage current of proposed device is 10^2 times lower than conventional one at 0V gate bias. As the gate bias is decreased negatively, the leakage current of conventional TFT significantly increases but that of the proposed one slightly increases. The ON/OFF current ratio of proposed poly-Si TFT was 10^6 while that of conventional one was 10^5.

Fig. 4 shows the transfer characteristics of the proposed poly-Si TFT's with various lengths of the amorphous region. We can see that as the amorphous region is longer, the leakage current decreases much more. However, the ON characteristics deteriorate with the length of amorphous region. Considering the leakage current of the new device with 1.2 ㎛ amorphous region is nearly the same as that of the new device with 1 ㎛, we can see that there is the saturation point to reduce the leakage current. In this figure, we conclude that the optimum length of amorphous region is about 0.5 ㎛.

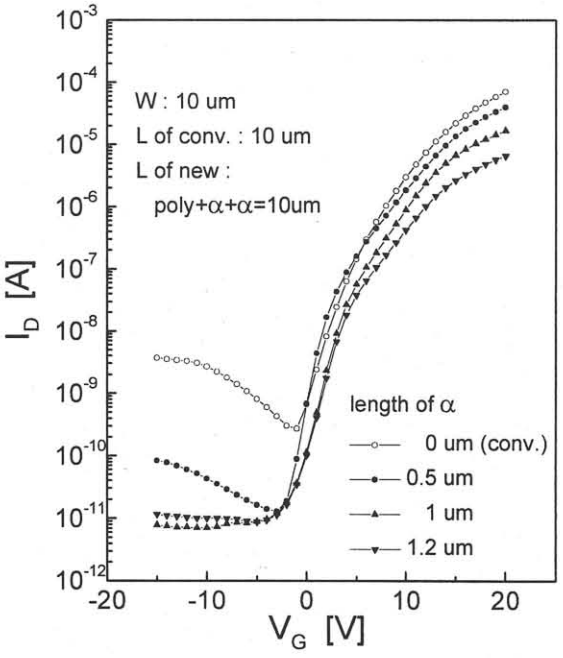

Fig. 4 The comparison of transfer characteristics of the new devices with the various lengths of amorphous region

5. Conclusion

We proposed the new poly-Si TFT structure which reduces the leakage current remarkably adopting the high resistance of a-Si. However the new device exhibits large on-current of poly-Si TFT. In the fabrication of the proposed device, there is not misalign problem because we employ the backlight exposure and photo resistor reflow process maintaining self-alignment. As we adopt the transparent ITO gate, we may design the pixel element to transmit more backlight of LCD pannel. Consequently, the aperture ratio may be increased.

References

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