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Differentiation of Effects Due to Grain and Grain Boundary Traps in Laser Annealed Poly-Si Thin Film Transistors

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Introduction

A new physical model based on two dimensional simulation for high quality laser annealed poly-Si thin film transistors is presented here. Electrical transport in poly-Si in general is modelled either by modulation of potential barriers at the grain boundaries [1] or else by assuming a uniform distribution of traps [2] throughout the material. These two approaches have been found to be suited to fitting characteristics of low quality material with a large number of defects and low mobility. Lately, laser re-crystallised, high quality poly-Si tfts with improved mobility (>100 cm^2 (Vs^{-1}) and subthreshold slope (< 0.5 V/decade) have been fabricated [3]. These tfts show marked difference from their predecessors in that they exhibit a distinct lack of saturation in their output characteristics. The two conventional modelling techniques have been found to be inadequate for these devices. It has been shown that in order to adequately explain both the improved subthreshold slope and the lack of saturation of the on-state characteristics, it is essential that the physical model must differentiate and include the effect of traps in grains and grain boundaries. Using fits to measured subthreshold slope and the output characteristics of poly-Si tfts with varying gate lengths, appropriate coefficients of a double exponential trap distribution for both grains and grain boundaries have been determined separately.

Modeling and Simulations

Figure 1 shows the effect of relative change in grain and the grain boundary trap density, respectively, on the threshold voltage (V_T) and the subthreshold slope (S). As a reference, unity on the x-axis scale represents the best fit combination for the respective trap density. It can be seen that the subthreshold slope is mainly dependent on the density of traps in grains for a fixed grain boundary trap density, while threshold voltage is more sensitive to the grain boundary trap density. It has been found here that only by determining the correct balance of traps in the grains and the grain boundaries is it possible to fit the correct subthreshold slope, the threshold voltage and the lack of saturation in the on-state characteristics. Figure 2 shows such an overall fit to subthreshold and the on-state characteristics for a 6 micron transistor. These fits have been used to quantifying the double exponential density of states distribution both in grains and grain boundaries (see Table I). It can be seen from the fit to the on-state characteristics that there is a discrepancy at high gate and drain voltage. At high gate voltage the measured characteristics show no evidence of impact ionisation and such is the trend that eventually a "negative resistance" region has been observed, particularly in devices with short gate lengths. This effect, similar to the mechanism observed in fully depleted SOI transistors, is associated with reduced mobility due to carrier heating [4]. It arises in laser annealed tfts because the glass substrate has a lower thermal conductivity than silicon, and devices exhibit higher values of carrier mobility and hence increased power dissipation.

Table I Trap distribution parameters for grains and grain boundaries used to fit characteristice of figure 2. N_{T1}, E_1 and N_{T2}, E_2 represent fitting parameters for deep states and tail states, respectively.

Grains (cm^{-3} eV^{-1})		Grain boundaries (cm^{-2} eV^{-1})		Exponential decay parameters	
N_{T1}	N_{T2}	N_{T1}	N_{T2}	E_1	E_2
$1x10^{18}$	$2x10^{19}$	$1.5x10^{13}$	$4x10^{14}$	0.23	0.038

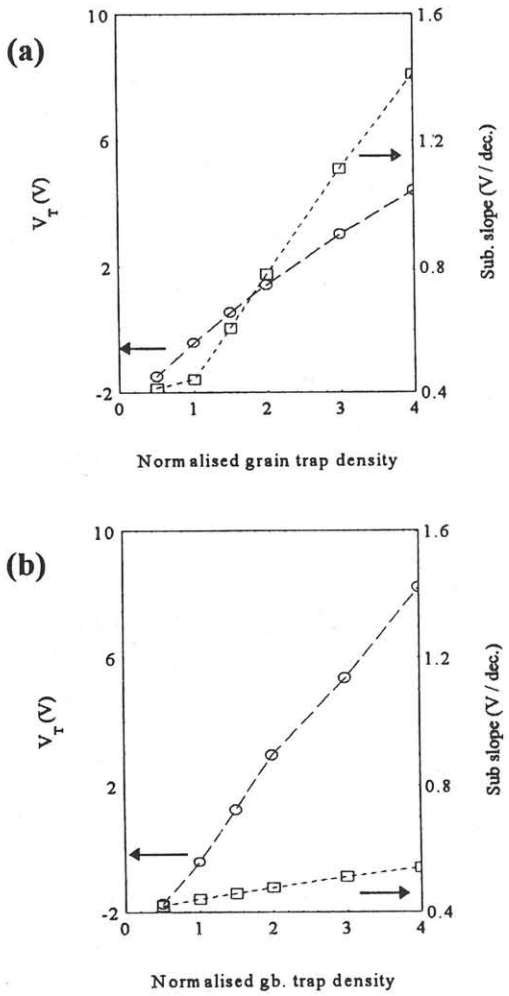

Figure 1 Effect on threshold voltage and subthreshold slope of (a) grain trap density and (b) grain boundary trap density.

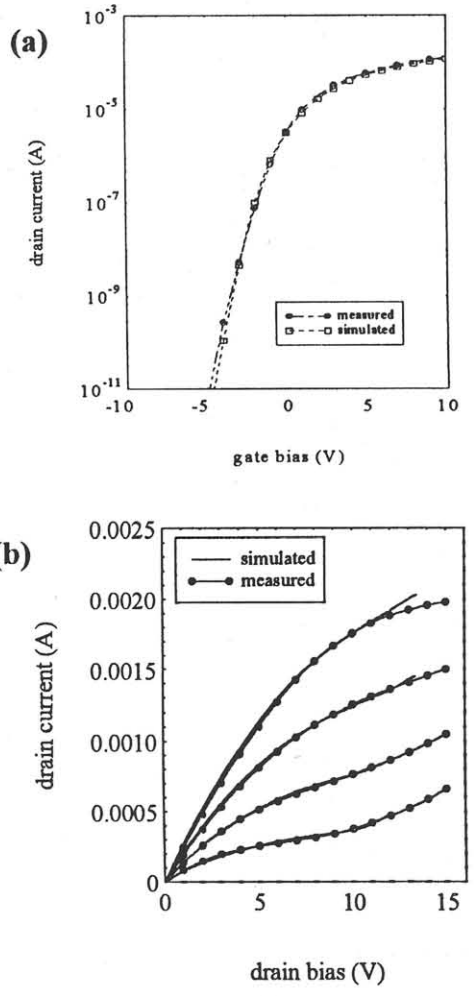

Figure 2 Fit to a 6 micron laser annealed poly-Si tft (a) subthreshold characteristics, V_d = 0.5V (b) on-state characteristics, V_g = 2V to 8V in steps = 2V.

References

1. C. A. Dimitriadis and D. H. Tassis, J. Appl. Phys., 2177 77 1995.
2. T-J. King, M. G. Hack and I-W. Wu. J. Appl. Phys., 908 75 1994
3. M.J. Edwards, S. D. Brotherton, J. R. Ayres, D. J. McCullough and J. P Gowers, Proc. Asia Display '95, Japan, 335, 1995.
4. M. Berger and Z. Chai, IEEE Trans. Elect. Dev., 38, pp. 871-875. 1991.