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Fabrication of Gate Overlapped-LDD poly-Si TFT for Large Area AMLCD

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1. Introduction

The anomalous leakage current of poly-Si TFTs is one of the key issues for the active matrix liquid crystal display (AMLCD) application[1]. In order to reduce the leakage current, we have proposed a new gate-overlapped (GO) LDD poly-Si TFT, of which the leakage current is decreased significantly while the ON current is not decreased[2]. In the previously reported GO-LDD poly-Si TFT, however, the ion implantation process and the impurity activation process of an implanted impurity are not suitable for large area AMLCD because the uniformity is decreased significantly. In this work, we have proposed the new fabrication methods of GO-LDD TFT without a troublesome ion implantation.

We have fabricated the GO-LDD TFT by employing the ion shower doping and *in-situ* doping which are the most promising techniques for the uniform doping on the large area glass substrate. In the GO-LDD TFT fabricated with *in-situ* doped source and drain (Fig. 1b), the electron-rich layer which behaves an LDD, can be formed by the accumulation of H^+ atoms during hydrogenation. Especially, this structure may be easily fabricated by the laser annealing and PECVD n+ a-Si:H layer, which are almost compatible with the fabrication process of the commercial a-Si:H TFT-LCD so that the low cost and large area application may be obtained.

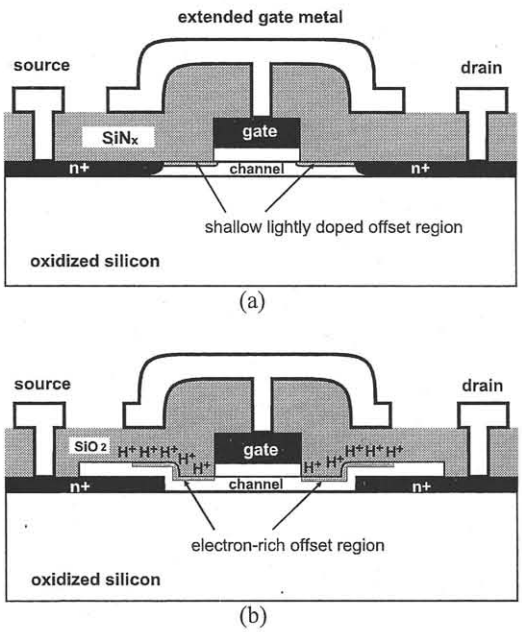

Fig .1 Cross-section of gate-overlapped lightly doped drain (GO-LDD) TFTs (a) with ion shower doping (b) with *in-situ* doped source and drain.

2. Device Fabrication

The fabrication process of ion-shower doped GO-LDD TFTs is almost identical to those of ion-implanted GO-LDD TFTs except PH_3/H_2 ion shower doping[1]. In the case of GO-LDD TFTs with *in-situ* doped source and drain, the 100 nm-thick phosphorous doped a-Si and 400 nm-thick TEOS interlayer are deposited by LPCVD and PECVD, respectively. The hydrogenation is performed by pure hydrogen plasma at 300 ℃ and 0.5 Torr in the commercial PECVD chamber.

3. Experimental Results

The measured I_D-V_G characteristics of the new GO-LDD TFTs with 270 Å-thick buffer oxide by employing ion shower doping is shown in Fig. 2. The leakage current of the new TFT is lower by the magnitude of two orders than that of non-offset devices at V_G=-20V without sacrificing the ON current. This lower leakage current of new TFT than that of conventional LDD TFT may be due to the more effective suppression of carrier emission via trap states, which is mainly caused by the remarkable reduction of peak vertical electric field due to the existence of field plate over the offset region. On the other hand, the ON current of new TFT is more significantly improved than that of conventional LDD TFT because of reduction of series resistance by the additionally induced electrons in the offset region.

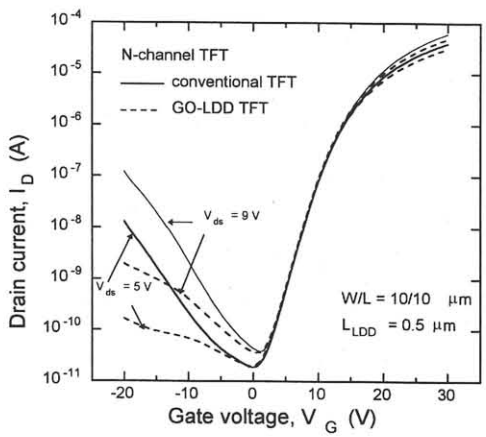

Fig. 2 The I_D-V_G curves of the new GO-LDD TFTs with 270 Å-thick buffer oxide by employing the ion shower doping. The thickness of SiN_X interlayer is 6000 Å.

Fig. 3 shows the I_D-V_G characteristics of the ion shower doped GO-LDD TFTs as a function of buffer oxide thickness.

The ON currents of GO-LDD TFTs are almost identical with the conventional non-offset TFT regardless of buffer oxide thickness because the amount of electron carriers in the LDD region may be determined by the extended gate voltage rather than the initial doping concentration.

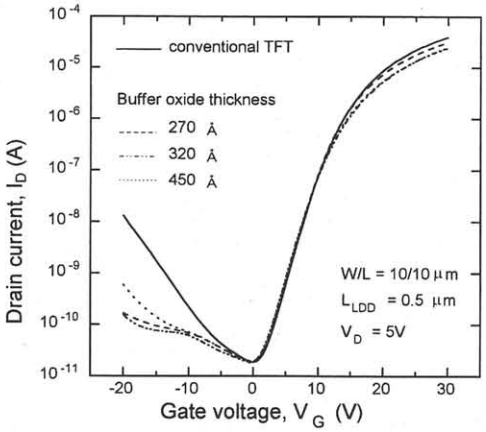

Fig. 3 The I_D-V_G curves of the new GO-LDD TFTs with 6000 Å-thick SiN_X interlayer as a function of buffer oxide thickness.

Fig. 4 shows that the ON/OFF current ratios of GO-LDD TFTs with *in-situ* doped source and drain are increased by more than the magnitude of three orders compared with those of conventional TFTs. After 4 hr hydrogenation, the electron-rich offset region formed by the H^+ accumulation and gate-overlap-structure reduce significantly the series resistance of offset region so that the ON currents of GO-LDD TFTs are almost identical to those of conventional non-offset TFTs.

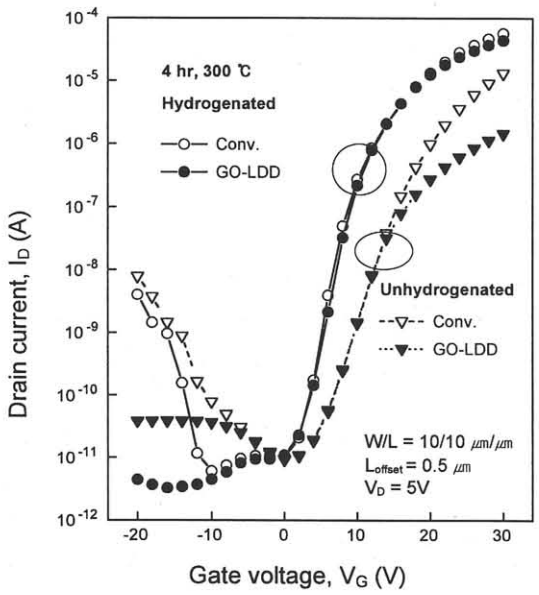

Fig. 4 The I_D-V_G curves of conventional non-offset TFT and GO-LDD TFT with *in-situ* doped source and drain before and after 4 h hydrogenation.

The decrease of leakage current of GO-LDD TFT may be caused by not only the effective suppression of hole accumulation in the offset region due to the GO-structure but also the significant reduction of trap-state density in the offset region due to the explosive hydrogen diffusion. The significant hydrogen diffusion in the offset region may be explained by that the amount of the diffused hydrogen atoms is strongly determined by the pathway oxide thickness. As the hydrogenation time is increased, the ON/OFF current ratio is increased significantly as shown in Fig. 5. The decrease of leakage current is saturated within 90 min while the increase of ON current is not saturated within 4 hr. The hydrogenation period may be much shorter in the offset region than in the active channel region because in case of the active channel region, the diffusion of H^+ atoms may be severely limited by the thin gate oxide. After gate bias stressing, the hydrogenated GO-LDD TFT with in-situ doped source and drain have not exhibited any degradation in the device characteristics due to the high quality TEOS SiO_2 interlayer.

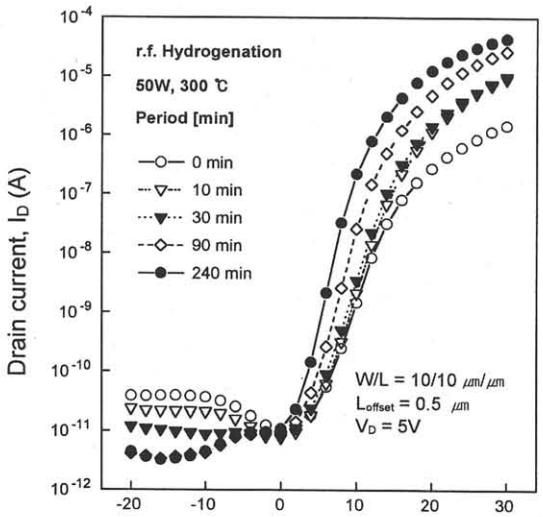

Fig. 5 The I_D-V_G curves of the GO-LDD TFT with *in-situ* doped source and drain as a function of hydrogenation period.

4. Conclusion

We have proposed and fabricated a GO-LDD poly-Si thin film transistor with high ON/OFF current ratios by employing the uniform doping techniques on the large area glass, such as ion shower doping and in-situ doping.

References

1) K.Y. Choi and M.K. Han : IEEE Electron Device Lett. **17**, (1996) p. 566
2) J.G. Fossum, A.O. Conde, H. Shichijo and S.K. Banerjee : IEEE Trans. Electron Devices **32** (1985) p. 1878.