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Dry Thermal Oxidation of Polycrystalline and Amorphous Silicon Films for Application to Thin Film Transistors

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1. Introduction

The improvement of polycrystalline silicon thin film transistors (p-Si TFTs) remains an important research area. At present p-Si TFTs are fabricated by basically the same process as are LSI devices, except for the thermal oxidation of polycrystalline silicon (p-Si) or amorphous silicon (a-Si) films to form polycrystalline semiconductor and gate insulator layers. The recent trend towards larger substrate requires lower processing temperatures, while maintaining TFT electrical properties equivalent to those fabricated at temperatures over 1100° C. Therefore, this paper studies the effects of oxidation temperature on the dry thermal oxidation of p-Si and a-Si films and will reveal how to improve the electric properties of the p-Si TFTs processed below 1000° C.

2. Experiment

Low pressure chemical vapor deposition (LPCVD) is used to prepare polycrystalline silicon (p-Si)[1] and amorphous silicon (a-Si)[2] films on fused quartz substrates at 600° C and 510° C, respectively. When TFTs are fabricated, the as-deposited films are patterned into islands. Prior to the thermal oxidation, the substrates are cleaned in boiling HNO_3 solution and dipped into 1.67% HF acid for 20 seconds. Immediately after natural oxide removal from the films, oxide films are grown to a thickness of 120 nm in 1 atm dry oxygen ambient at temperatures between 900° C and 1160° C. After the oxidation, the silicon films are reduced in thickness to about 30 nm.

Using the polycrystalline semiconductor and oxide layers, n-channel p-Si TFTs are fabricated through a standard high-temperature process.[1,2] Thickness and refractive index are measured by spectroscopic ellipsometry. The p-Si/SiO_2 interface is observed by scanning electron microscopy (SEM).

3. Results

Figure 1 shows the dependence of mobility on the oxidation temperature. The temperature of 1070° C is a break point, below which mobility values dramatically decrease as oxidation temperature decreases. The dependence is especially strong for the p-Si TFTs obtained by p-Si oxidation. These devices always show inferior electrical characteristics compared to those obtained by a-Si oxidation.[2]

The mobility dependence is explained by the different conditions of the p-Si/SiO_2 interface. SEM photographs of the interface are presented in Fig. 2, and indicate that high temperature oxidation produces a smooth interface but low temperature oxidation produces a rough interface. The rough interface is especially pronounced for low temperature oxidation of p-Si films, resulting in poor mobility values.

The refractive index of the oxide is shown in Fig. 3. The break point temperature is again 1070° C. Below this temperature, the refractive index of the oxide increases as the oxidation temperature falls. Oxide obtained by p-Si oxidation has an abnormally strong dependence of refractive index on the oxidation temperature.

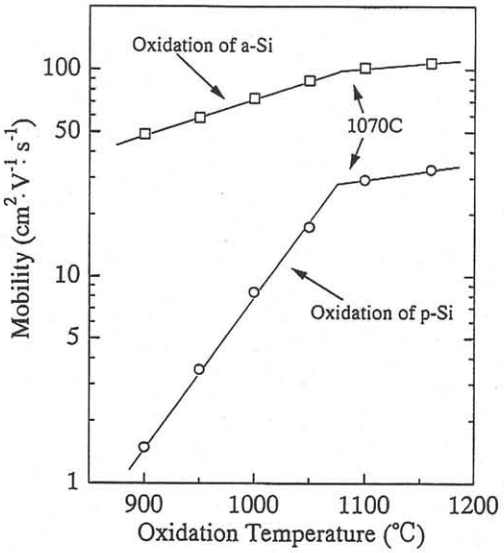

Fig.1 Mobility dependence.

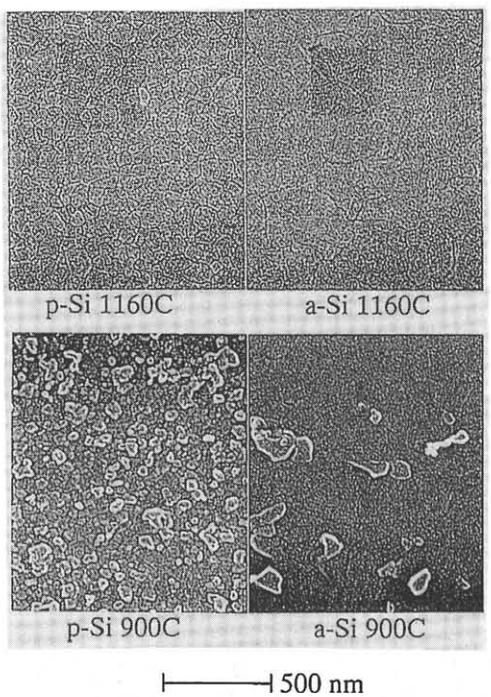

Fig. 2 SEM photographs of the interface.

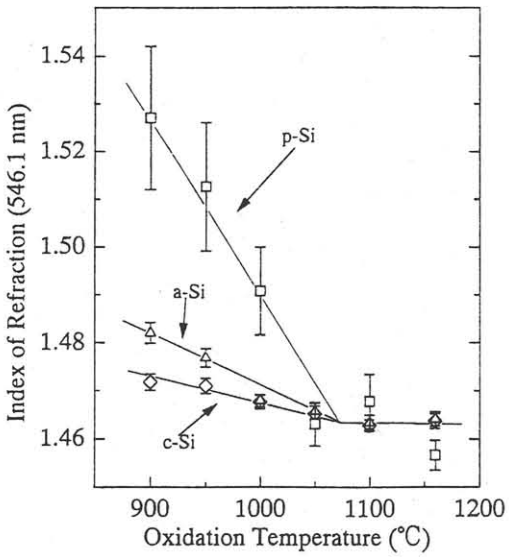

Fig. 3 Refractive index of the oxide.

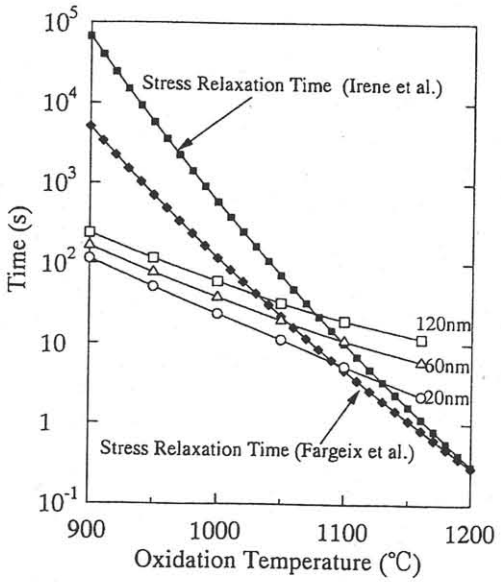

Fig. 4 Oxdation time and relaxation time.

4. Discussion

It is well-known that the dry thermal oxide of single crystal silicon (c-Si) grown at low temperature has a large value of refractive index[3-4] and that the increase of the refractive index is attributable to the presence of intrinsic oxidation stress.[5] The strong intrinsic stress is known to cause a silicon horn at the Si/SiO_2 interface of the convex corner.[6] Although the reason is not clear, p-Si oxidation induces very strong stress (Fig. 3). In addition, as-deposited p-Si surface is not flat but possesses many natural convex corners, because of presence of grains and grain boundaries. These two facts combine to seriously damage the interface (Fig. 2). As a result, the corresponding p-Si TFTs show poor electrical characteristics (Fig. 1). Since the stress generated during a-Si oxidation is not very strong and since the as-deposited a-Si surface is rather flat, the interface condition and mobility for a-Si oxidation do not depend on the temperature as strongly as they do for p-Si oxidation.

The temperature break point is explained by the relationship between oxidation time and stress relaxation time. Various researchers have considered SiO_2 as a viscous solid to calculate the stress relaxation time,[7-9] which is drawn in Fig. 4. Figure 4 also presents one-atomic-layer oxidation time, which is the time needed to oxidize one more silicon layer at an adequate oxide thickness, based on a classical Deal-Grove model.[10] At 1160° C the stress relaxation time is shorter than the one-atomic-layer oxidation time for the entire oxidation period. Therefore, the stress is always relaxed at the growing oxide front, resulting in a smooth interface. On the other hand, at temperatures below 1000° C the relaxation time is always longer than the oxidation time. As a result, oxide grows under a stressed condition and the interface becomes rough. The cross-over point between the two curves of stress relaxation time and oxidation time corresponds to the temperature break point, which is observed clearly.

In the case of c-Si oxidation, inert-gas annealing at high temperature removes the negative effects of low temperature oxidation, such as high values of refractive index, density, stress, fixed oxide charge and interface trapped charge, because these negative effects are due to the intrinsic oxidation stress which can be relaxed by the inert-gas annealing at high temperature.[11-12] In the case of p-Si or a-Si oxidation, even if inert-gas annealing removes the stress, a rough interface remains. Inert-gas annealing does not convert rough interfaces to smooth ones. Therefore, it is important for fabricating good TFTs that p-Si or a-Si films are oxidized under the condition that the relaxation time is shorter than the oxidation time, so as to keep the interface free from stress.

5. Conclusion

Silicon oxidation involves the temperature break point, which results from a relative magnitude between the stress relaxation time and the one-atomic-layer oxidation time. When p-Si is oxidized below the break point temperature, the $p\text{-}Si/SiO_2$ interface is roughened during oxidation by the astonishingly strong stress and the presence of grains. The rough interface degrades mobility in the polycrystalline semiconductor devices.

In order to fabricate good p-Si TFTs, the following two conditions should be satisfied.

(1). Amorphous silicon must be oxidized rather than p-Si.

(2). The one-atomic-layer oxidation time must always be longer than the stress relaxation time.

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