Improvement of Reliability of MOSFET's with N_2O Nitrided Gate Oxide and N_2O Polysilicon Gate Reoxidation

Chao Sung Lai, T. S. Chao, Tan Fu Lei', Cheng Len Lee', T. W. Huang, C. Y. Chang'

National Nano Device Laboratory, Hsinchu, Taiwan, R. O. C.

Phone : 886-3-5726100, Fax : 886-3-5713403, E-mail : cslai@ndl.nctu.edu.tw

¹Department of Electronics Engineering, National Chiao Tung University Hsinchu, Taiwan, R. O. C.

1. Introduction

The hot electron reliability is correlated to the gate oxide integrity near the polysilicon gate edge [1]. A damage phenomenon, edge damage, occurred near the drain and source junctions during gate polysilicon plasma etching [2]. It was reported that N₂O oxynitride poly-gate reoxidation process is effective in suppressing the reverse short channel effect (RSCE) without degradation the short channel behavior of the MOSFETs [3]. Therefore, polysilicon gate sidewall reoxidation is important for improving gate oxides. Recently, it is found that N₂O nitrided gate oxide is more robust than O₂ gate oxide in resisting the process-induced degradation. Also, to grow a thin oxide on the polysilicongate in N₂O ambient lessens the degradation on the underlying gate oxide than to grow it in O₂ ambient[4].

In this work, firstly, the electrical characteristics of MOSFETs with N_2O nitrided gate oxide and processed by N_2O poly-gate reoxidation have been investigated, including hot electron immunity, RSCE, interface generation and antenna effect.

Table I	The	preparation	sequences	for	this	work.
---------	-----	-------------	-----------	-----	------	-------

Devices	Gate Dielectrics Wet Oxidation N ₂ O annealing		Poly-Si gate	poly-Sigate(WSix) re-oxidation	
ON ₀₀ PO	√	-	~	- ₍₀₂)	
on ₀₀ pn	V .	-	V	√ (N ₂ O)	
ON 20PO	V	√(20 min)	v	— (O ₂)	
ON 20PN	~	√(20 min)	\checkmark	√ (N ₂ O)	
on ₄₀ po	V	√(40 min)	\checkmark	— (O ₂)	
on ₄₀ pn	V	√(40 min)	~	√ (N ₂ O)	
on ₆₀ po	V	√(60 min)	~	_ (O ₂)	
ON:60PN	~	√(60 min)	√	√ (N ₂ O)	

2. Experiments

N⁺ polysilicon-gate n-MOSFET's with different gate oxides were fabricated using a 0.35 μ m CMOS process. The O₂ gate oxide was grown in wet-oxidation at 800 °C and then annealed in N₂ at 900°C. For comparison, the N₂O nitrided oxide was firstly grown in wet-oxidation at 800 °C followed by N₂O annealing at 850°C for 20 to 60 min to control the final thickness of 8.5 nm. For the poly-Si gate reoxidation process, there are two groups, one is reoxidized in O_2 ambient (O_2 poly-reoxidation) and the other in N_2O ambient (N_2O poly-reoxidation) at 850 °C for 20 min.

The preparation sequences for these samples were summarized in Table I. For example, the O_2 oxide sample with O_2 poly-reoxidation is denoted as $ON_{00}PO$. For the 40 min N_2O nitrided oxide with N_2O poly-reoxidation is denoted as $ON_{40}PN$.

3. Results and Discussion

Hot carrier immunity was investigated which devices were biased at peak value of substrate current under constant drain voltage (V_d =5V). Fig 1 (a) and (b) show the hot carrier induced transconductance (g_m) degradation for O_2 and N_2O poly-reoxidation, respectively.



Fig. 1 The hot carrier stress induced g_m degradation for (a) O₂ and (b) N₂O poly-reoxidation, respectively.

We can find that degradation is decreased as increasing N_2O nitrided time. This reduction in g_m degradation was mainly due to a reduction in interface generation under stress. Comparing to O_2 poly-reoxidation samples (solid line), N_2O poly-reoxidation sample (dotted line) had much improved hot carrier immunity. Measurement of the charge pumping current , I_{cp} , was carried out as shown in Fig. 2 which the repetition frequency and width of the gate pulse were 100 kHz and 5μ s, respectively. 2000



Fig. 2 Charge pumping current, Icp, for all samples.

It showed that $ON_{60}PN$ had the smallest I_{cp} after hot carrier stress. This meant that $ON_{60}PN$ has the smallest generation of interface state density. This was consistent with the result of g_m degradation as shown in Fig. 1.

The RSCE was studied as shown in Fig. 3 (a) and (b) for O_2 and N_2O poly-reoxidation, respectively.



Fig. 3 The treshold voltage virsus channel length (a) O_2 and (b) N_2O poly-reoxidation, respectively.

It can be seen that the RSCE was suppressed, not only for N_2O nitrided oxides but also N_2O poly-reoxidation process. As increasing N_2O annealing time, the RSCE was decreased. Due to the incorporated nitrogen at the oxide/Si-substrate interface which retarded the poly-reoxidation enhanced channel boron diffusion, resulted in uniform channel boron distribution.

We use F-N tunneling leakage current and charge-tobreakdown (Q_{bd}) of gate oxides to monitor the plasma charging induced degradation on all samples. Antenna effects on gate leakage current were shown in Fig. 4.



Fig. 4 The effect of plasma charging on gate leakage current with various atenna ratio for all samples.

It shows that leakage current is increased by increasing antenna ratio. However, as increasing N_2O nitrided time, the leakage current due to antenna effects was decreased. The leakage current is slightly increased as increasing antenna ratio for all samples with N_2O poly-reoxidation.

The Q_{bd} under 100 mA/cm² F-N stressing with different antenna ratio was shown in Fig.5 (a) and (b) for O_2 and N_2O poly-reoxidation, respectively. When the antenna ratio was increased, the Q_{bd} was decreased for all samples with poly- O_2 reoxidation. Fortunately, the Q_{bd} is slightly decreased as increasing antenna ratio for all samples with N_2O polyreoxidation.



Fig. 5 The Qbd virsus antenna ratio for (a) O_2 and (b) N_2O poly-reoxidation, respectively.

4. Conclusion

A systematic study of the reliability of MOSFET's with N_2O nitrided gate oxides and processed by N_2O poly-gate reoxidation was presented. Combination of N_2O nitrided gate oxides and N_2O poly-gate reoxidation, hot electron immunity was improved and RSCE, interface generation, antenna effect on leakage current and Q_{bd} was suppressed.

References

- R. Rakkhit, F. P. Heiler, P. Fang and C. Sander: International Reliability Physics Symposium (IRPS), p.293, 1993.
- P. G. Y. Tsui, H. H. Tseng, M. Orlowski, S. W. Sun, P. J. Tobin, D. Reid, and W. J. Taylor: *IEDM Tech. Dig.*, p.501, 1994.
- S. Fang and J. Mcvittie: IEEE Electron Device Lett. vol.13, p.374, 1992.
- 4) C. S. Lai, T. F. Lei, C. L. Lee and T. S. Chao: *IEEE Electron Device Lett.* vol.16, p.407, 1995.