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New Insight into the Degradation Mechanism of Nitride Spacer with Different Post-Oxide in Submicron LDD MOSFET's

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1. Introduction

Recently, LDD MOSFET with silicon-nitride spacer has been widely used for 64/128MB DRAM design. Not only its self-align contact feature to increase the cell density, but also its high performance and reliability by using gate-fringing field effects [1][2]. On the other hand, the low-temperature chemical-vapor deposition (CVD) to grow the post-oxide beneath the nitride spacer is gradually accepted to replace the high thermal oxidation owing to the prevention of the silicide peeling and limited thickness by RTO. However, extra degradation of devices due to this low temperature process will occur. Therefore, in this paper, the hot-carrier degradation of devices with silicon-nitride spacer has been studied for various post-oxide structures. The stress induced oxide damages, including the interface state (N_{it}) and oxide charges (Q_{ox}), will be accurately determined to analyze the device reliability. In addition, the way to suppress the hot-carrier degradation will be suggested.

2. Device Fabrication

The devices used in this study were made by 0.5μm CMOS technology. The gate oxide thickness is 12nm. Three different types of post oxide with 20nm under the silicon-nitride spacer were formed and shown in Fig.1. Device 1 is the one with the post oxide formed by CVD only. Device 2 is also grown by CVD followed by annealing in the N_2 ambient for 30min 850°C. Device 3 is formed by 80Å thermal oxide residual after poly-gate etching and then grown 120Å CVD oxide.

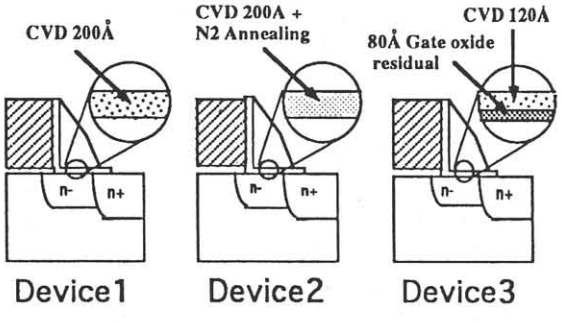

Fig. 1 Device structures used in this study. All of three devices have different post-oxides under the nitride spacer.

3. Results and Discussion

To study the hot carrier reliability of devices, the substrate current I_B and impact inoization rate (I_B/I_D) at different gate voltages are measured as shown in Fig. 2. Fig. 3 shows the drain current degradation ($\Delta I_D/I_D$) at maximum substrate current stress biases. By comparing both Figs. 2 and 3, it shows that Device 3 has the largest substrate current but its $\Delta I_D/I_D$ degradation is the smallest. This implied that there is another degradation factor in addition to the generated interface states. It is worth noting that the difference between these three devices is only the post oxide. Device 1 exhibits the shortest lifetime. Device 2 with CVD oxide and N_2 annealing has about the similar lifetime to that of Device 3. This amounts to say that a device with low temperature CVD oxide and appropriate annealing process (Device 2) can improve largely the hot carrier reliability.

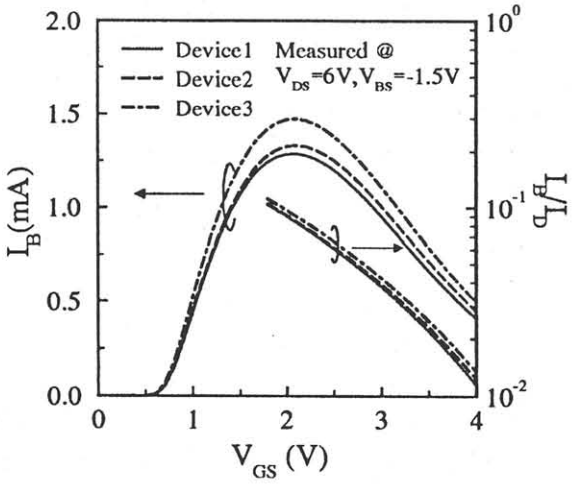

Fig. 2 Measured substrate currents and the impact ionization rate (I_B/I_D) for three devices.

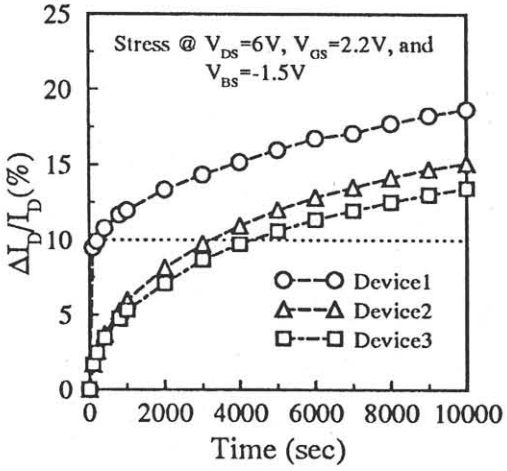

Fig. 3 Measured drain current degradation versus stress time for three devices under maximum substrate current stress.

To study the correlation between oxide damages and the device degradation, profiling of interface state and oxide trap

charge using an improved gated-diode current measurement by us in [3] is used. The results in Fig. 4 show the calculated interface states for all three devices. Device 3 has the largest ΔN_{it} but its $\Delta I_D/I_D$ degradation is the lowest. This shows further the evidence that the degradation of devices can not be judged purely from the generated interface states. Fig. 5 shows the GIDL current before and after 500sec stress, it indicates that there are Q_{ox} generated in the post-oxide during hot carrier stress [4].

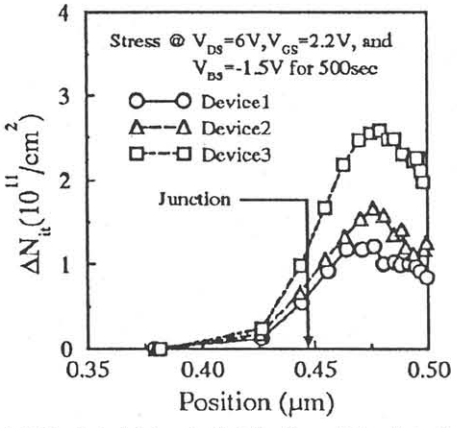

Fig. 4 Calculated lateral distribution of the interface states for three devices.

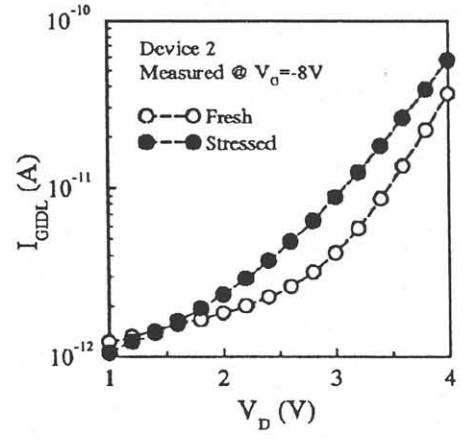

Fig. 5 Measured fresh and stressed GIDL currents of Device 2.

Fig. 6 shows the comparison of the extracted ΔN_{it} and ΔQ_{ox} for three devices under various stress times. We see that all three devices have similar ΔN_{it} distribution since they have similar drain structure. But, more importantly, the generated Q_{ox} has a large difference due to different structure of post-oxide for three devices. We can further calculate the individual contribution of ΔN_{it} and ΔQ_{ox} to the drain current. Again, Fig. 7 shows the results for Device 2, in which the contribution of the device degradation for Q_{ox} is much larger than that of N_{it}. It is concluded from Fig. 3 that Device 2 has approximately the same reliability as Device 3 (thermal oxide) and can be a successful process for low temperature CVD with appropriate annealing process.

4. Conclusion

In this paper, the hot-carrier degradation of LDD devices with silicon-nitride spacer was investigated for various post-oxide structure under the spacer. A method for calculating oxide damages was also developed. It was found that Q_{ox} generated in the post-oxide will dominate the degradation of devices with low temperature CVD process. The generated oxide charges can be successfully suppressed for the CVD oxide with appropriate N_2 anneal. Therefore, Q_{ox} must be taken into account for designing high density DRAM's with silicon-nitride spacer in LDD devices.

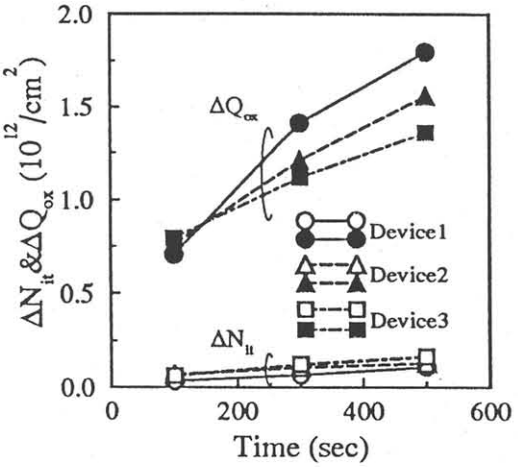

Fig. 6 Calculated total amount of oxide damages (interface state and oxide charge) for three devices.

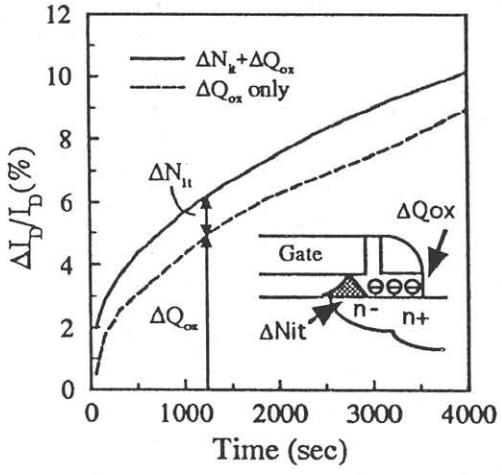

Fig. 7 Individual contribution of the interface state and oxide trap charge to the drain current degradation for Device 2.

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