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Temperature Effect on Off-State Drain Leakage Current in a Hot-Carrier Stressed n-MOSFET

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1. Introduction

It was reported that hot carrier stress generated interface traps can introduce an additional drain leakage current in an off-state MOSFET [1,2]. Previously, this phenomenon was attributed to the trap-related field effects such as trap-assisted sequential tunneling or enhancement of band-to-band tunneling due to the trapped charge build-up [2]. In addition to the field effects, recent experimental result showed that the trap-induced drain leakage exhibits a strong dependence on temperature at certain applied biases [3]. This leakage current becomes much aggravated as the temperature increases and thus may have impact on a DRAM refresh time. In this work, we intend to characterize and analyze the temperature effect on the trap-assisted drain leakage mechanisms in an off-state MOSFET.

2. Trap Assisted Drain Leakage Model

A complete trap-assisted drain-to-substrate leakage path at the Si/SiO_2 interface is formed by hole emission from interface traps to a valence band and electron emission from the traps to a conduction band. Both hole emission and electron emission can be carried out via field emission or thermionic emission. Fig. 1 illustrates four possible trap-assisted leakage paths.

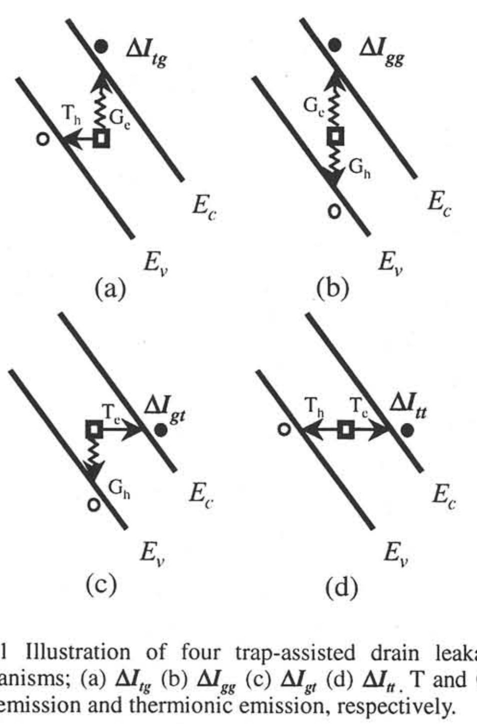

Fig. 1 Illustration of four trap-assisted drain leakage current mechanisms; (a) ΔI_{tg} (b) ΔI_{gg} (c) ΔI_{gt} (d) ΔI_{tt}. T and G represent field emission and thermionic emission, respectively.

In the figure, T_e and T_h denote electron tunneling and hole tunneling and G_e and G_h represent electron and hole thermionic emission. Note that ΔI_{gg} in Fig. 1(b) is the trap-assisted thermal generation current and ΔI_{tt} in Fig. 1(d) is the trap-assisted sequential tunneling current. The carrier transition rates for the various emission mechanisms are formulated below [1].

$$G_e = v_{th}\sigma_n\left[n_i exp\left(\frac{E_t - E_i}{kT}\right)f_t - n_s(1-f_t)\right] \quad (1)$$

$$G_h = v_{th}\sigma_p\left[n_i exp\left(\frac{E_i - E_t}{kT}\right)(1-f_t) - p_s f_t\right] \quad (2)$$

$$T_e = (f_t - f_c)/\tau_e \quad (3)$$

$$T_h = ((1-f_t)-(1-f_v))/\tau_h \quad (4)$$

where f_c, f_t and f_v are electron occupation factors in the conduction band, trap states and the valence band respectively. n_s and p_s are electron and hole concentrations at interface, which were calculated from a two-dimensional device simulation. τ_e and τ_h are electron and hole tunneling times evaluated from the WKB approximation. In a steady-state, f_t can be obtained from the equality $G_e+T_e=G_h+T_h$ with $f_c\approx 0$ and $f_v\approx 1$. The trap-assisted drain leakage current ΔI_d is therefore expressed in the following,

$$\Delta Id = qW\int_{\Delta L}\int_{Ev}^{Ec} Nit(Et,x)(Ge+Te)dxdEt \quad (5)$$
$$= \Delta Igg + \Delta Igt + \Delta Itg + \Delta Itt$$

where W is the channel width and ΔL is the length of the interface trap (Nit) region.

Other temperature-dependent parameters used in the calculation are band-gap(E_g), thermal velocity(v_{th}) and intrinsic concentration(n_i). They are given below [4];

$$E_g = E_g(T=0) - \alpha T^2/(T+\beta) \quad (6)$$

$$v_{th} = \sqrt{3kT/m^*} \quad (7)$$

$$n_i = \sqrt{N_c N_v}\exp(-Eg(T)/2kT) \quad (8)$$

3. Results and Discussions

In measurement, a 0.6μm conventional S/D n-MOSFET with 100Å gate oxide and 25μm gate width was used. The device was subject to maximum substrate current stress, V_{ds}=5.5V and V_{gs}=2.5V, for 2000 seconds at T=373K. Under the stress condition, the trapped charge induced interface field variation is small [2]. Fig. 2 shows the measured pre-stress and post-stress drain leakage currents at T=290K and 373K. The junction leakage current is about 5pA at T=373K and the drain-to-source leakage current is much smaller. The increased drain leakage current due to interface trap generation, ie. the difference between the pre-stress and the post-stress drain currents, is plotted in Fig. 3.

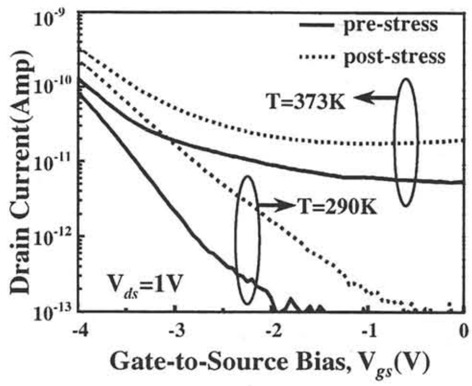

Fig. 2 Measured drain leakage current characteristics before and after stress at two different temperatures, T=290K and T=373K.

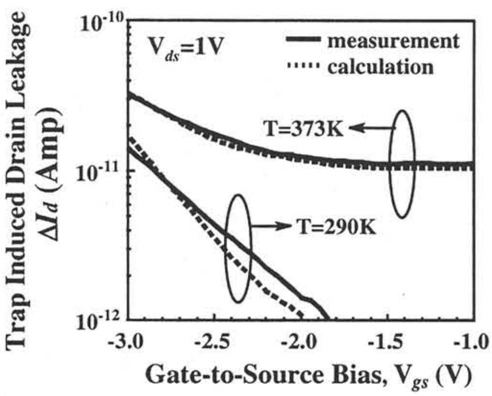

Fig. 3 Measured and calculated interface trap induced drain leakage currents at T=290K and T=373K.

The dash lines are calculated results. Apparently, the ΔI_d increases significantly with temperature at a small V_{gs} Furthermore, the V_{gs} dependence (field dependence) of the ΔI_d becomes relatively weak at T=373K, which indicates the increasing importance of the thermionic emission mechanism at the higher temperature. In order to further analyze the various drain leakage mechanisms, the four components of the ΔI_d were calculated in Fig. 4 (T=290K) and Fig. 5 (T=373K).

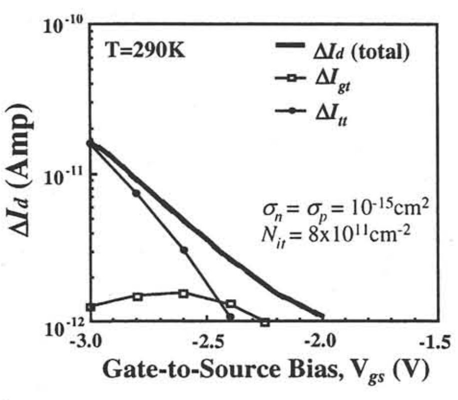

Fig. 4 Calculation of various drain leakage current components at T=290K. ΔI_{tg} and ΔI_{gg} are negligible in this figure

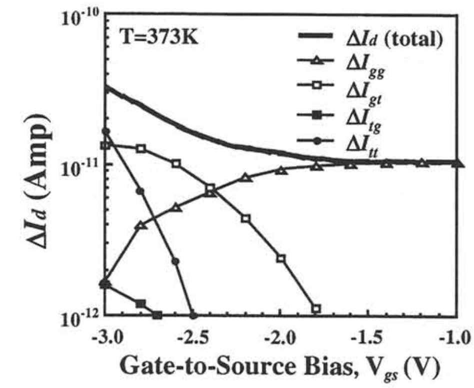

Fig. 5 Calculation of various leakage current components at T=373K.

In the calculation, the interface traps were assumed to have a uniform distribution in the bandgap. The trap density N_{it} we used is $8x10^{11}cm^{-2}$ and the length of the trap distribution in the channel (ΔL) is 400Å. $\sigma_n=\sigma_p=10^{-15}cm^2$ [4]. At T=290K, the drain leakage current is dominated by ΔI_{tt} for $|V_{gs}|>2.4V$ and by ΔI_{gt} for $|V_{gs}|<2.4V$. At the higher temperature, T=373K, the sequential tunneling component ΔI_{tt} is dominant for $|V_{gs}|>2.9V$. The thermionic-field emission component ΔI_{gt} holds responsible for $2.4V<|V_{gs}|<2.9V$ and the thermionic emission component ΔI_{gg} (above 10pA) appears to be a major leakage mechanism for $|V_{gs}|<2.4V$.

4. Conclusions

The interface trap induced drain leakage current was characterized and modeled at different temperatures for the first time. Our study shows that while the trap-assisted thermionic emission current is unimportant at room temperature, it appears to be a major drain leakage mechanism in a stressed n-MOSFET as the temperature increases.

Acknowledgments

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