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Short-Channel Effects in N- and P-Channel Polysilicon Thin Film Transistors with Very Thin ECR N_2O-Plasma Gate Dielectrics

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1. Introduction

In recent years, many of researches are concentrated on reducing the channel dimension of poly-Si TFT's for high integration [1],[2]. However, as the channel length is reduced, poly-Si TFT's are subjected to more severe short-channel effects in comparison with bulk-MOSFET's [2]. It was known that using thin gate oxide in poly-Si TFT's suppresses short-channel effects [3] and make low-voltage operation possible [4]. However, because growing a high quality thin gate oxide on poly-Si is very difficult so far, short-channel effects in poly-Si TFT's with thin gate oxide have not been fully investigated.

In this work, we investigated short-channel effects in n- and p-channel poly-Si TFT's using a high quality very thin (12nm) ECR N_2O-plasma oxide as a gate dielectric and compared the results with using thermal gate oxide.

2. Experiments

Complementary poly-Si TFT's were fabricated on thermally oxidized silicon wafers using SPC method. A 12nm-thick ECR N_2O-plasma oxide was grown at 400°C with a microwave power of 600W. For comparison a 9.7nm-thick thermal oxide was grown at 900°C in dry O_2. Gate and S/D regions were doped with $Ph.^+$ (BF_2^+) implantation with a dose of $5\times10^{15}cm^{-2}$ for n-channel (p-channel), followed by annealing at 900°C in N_2. Some of samples were hydrogenated in ECR apparatus at 300°C with 600W.

3. Results and Discussion

Fig. 1 and 2 show the I_D-V_G transfer characteristics of n- and p-channel TFT's, respectively. The measured device parameters are summarized in Table I. N_2O-TFT's show higher mobilities and lower minimum leakage currents in comparison with thermal-TFT's for both n- and p-channel cases. It was found that N_2O-plasma oxidation does not degrade surface of poly-Si resulting smooth interface, leads to higher mobility [4]. In addition, defects in the grain boundaries are passivated during N_2O-plasma oxidation [4]. The improved performance of hydrogenated N_2O-TFT's are due to lower trap density of channel poly-Si film.

Fig. 3 shows the normalized threshold voltage versus channel length (L). The shift is larger at higher drain bias. The more severe shift in n-channel TFT's, particularly at high drain bias, are attributed to the higher ionization rate of electrons in comparison with holes, leads to enhanced channel avalanche multiplication [2]. The hydrogenated devices exhibit severe shift, especially for n-channel device, suggesting higher charge accumulation in active poly-Si [3].

It should be noted that, in spite of thicker oxide, N_2O-TFT's exhibit smaller shift in comparison with thermal-TFT's; this is considered to be due to the role of nitrogen atoms. In our secondary ion mass spectroscopy (SIMS) measurement, N_2O-plasma oxide has a nitrogen-rich layer at the interface. Fig. 4 shows the X-ray photoelectron spectroscopy (XPS) intensity of N(1s) at the interface. The N(1s) energy of 397.8eV reveals that the oxynitride layer contains strong Si ≡ N bonds [4]. Therefore, we can infer that Si ≡ N bond has strong immunity under impact ionization, resulting smaller shifts of N_2O-TFT's at high V_D.

Fig. 5 shows that subthreshold slope is reduced as L is decreased; this is attributed to the charge accumulation in poly-Si film by impact ionization [2]. The severe reduction in hydrogenated devices reveals that the lower trap density makes the devices more sensitive to the effect of charge accumulation [3]. The abrupt increase of slope in hydrogenated device at L = 1μm is due to punchthrough.

The leakage current in short-channel device is related not only drain induced barrier lowering but also channel electric fields Fig. 6 shows that minimum off-state leakage current is rapidly increased as L is reduced blow 5μm for both n- and p-channel cases. Fig. 7 shows that the punch-through voltages (V_{PT}) is decreased as L is reduced below 3μm in n-channel TFT's, while kept roughly constant in p-channel TFT's. Thus, in n-channel devices, the increase of leakage current is due to the increase of channel electric field (L>3μm) and drain induced barrier lowering (L<3μm). However, in p-channel devices, the increase of leakage current is mainly attributed to the increase of channel electric field in all range of channel lengths.

4. Conclusions

Short-channel effects in n- and p-channel poly-Si TFT's with high quality very thin ECR N_2O-plasma gate oxide were investigated. It was found that nitrogen-rich layer at the interface containing Si ≡ N bonds, which has good immunity under impact ionization, suppressing the short-channel effects. Charge accumulation by impact ionization is mainly responsible for the short-channel effects.

In addition, the results on low voltage operating circuits will be presented.

References

1) N. Yamauchi, et. al., in *IEDM Tech. Dig.*, p. 353, 1989.
2) S. Yamada, et. al., in *IEDM Tech. Dig.*, p. 859, 1990.
3) A. G. Lewis, et. al., in *IEDM Tech. Dig.*, p. 349, 1989
4) J. W. Lee, et. al., *IEEE EDL*, May, 1997, to be published.

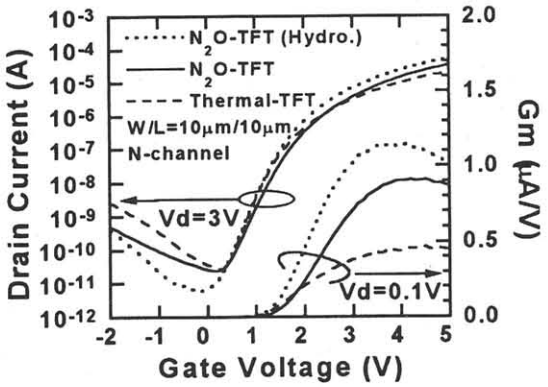

Fig. 1 Id-Vg transfer characteristics of n-channel TFT's

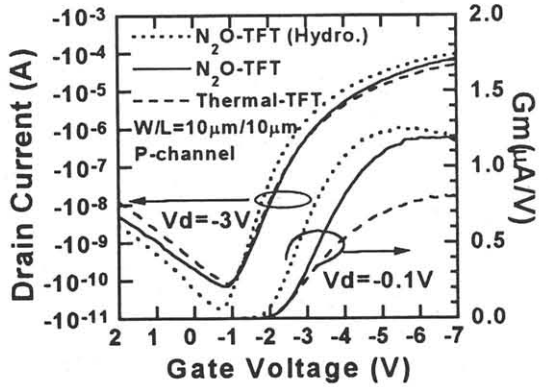

Fig. 2 Id-Vg transfer characteristics of p-channel TFT's

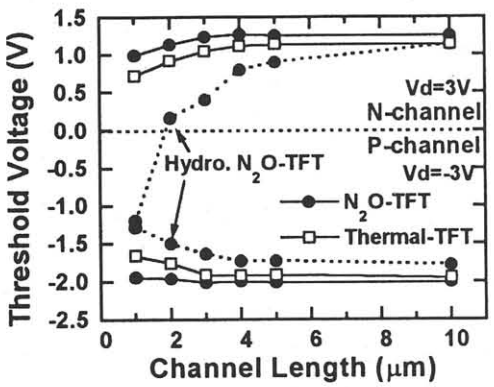

Fig. 3. Threshold voltage versus channel length for n- and p-channel TFT's. Threshold voltage is measured at a constant current with I_{DS}=10nA at and 3V.

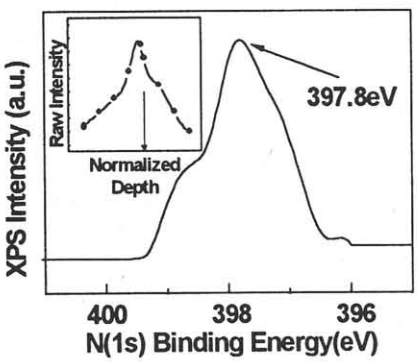

Fig. 4. XPS N(1s) intensity of N_2O-plasma oxide at the interface. Inset : depth profile of N(1s) intensity.

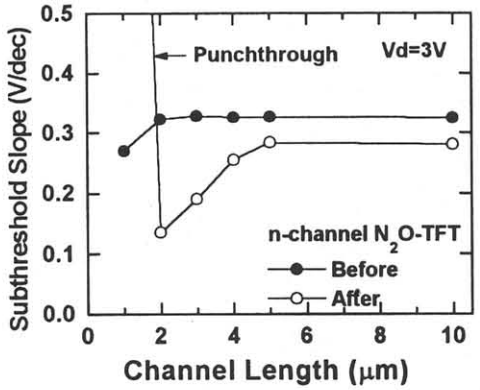

Fig. 5. Channel length versus subthreshold slop of n-channel N_2O-TFT's before and after hydrogenation.

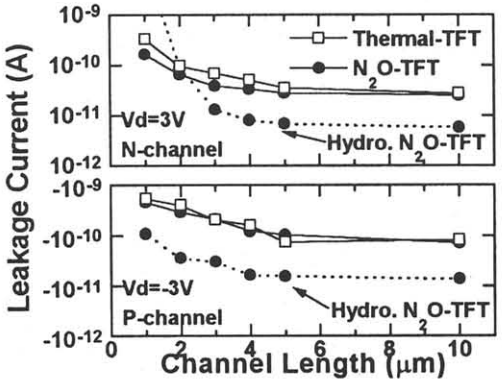

Fig. 6. Off-state leakage current versus channel length for n- and p-channel TFT's.

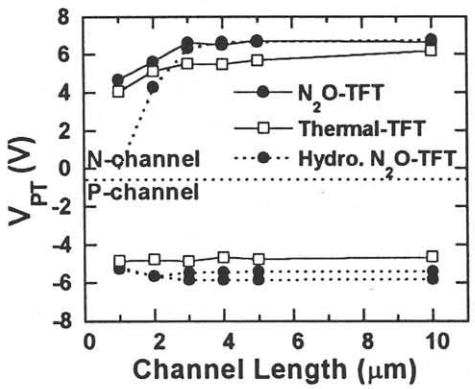

Fig. 7. Punchthrough voltage versus channel length for n- and p-channel TFT's. V_{PT} defined as a V_{DS} where I_D reaches |10nA| at V_{GS}=0V.

Table I. Summary of device parameters. Device size is W/L=10μ/10μ. Threshold voltage is measured at Ids=10nA at Vds=0.1V. On/Off current ratios are for the gate voltage swing of ~5V for n-channel and ~7V for p-channel.

	Type		Vt	μ	S	Imin	On/Off
Thermal	N-ch		1.27	13.0	0.27	27.2	0.78
	P-ch		-2.15	22.8	-0.46	-81.6	0.63
N_2O	Un-hydro.	N-ch	1.40	31.7	0.32	24.7	1.44
		P-ch	-2.18	41.4	-0.44	-72.2	1.01
	Hydro.	N-ch	1.25	39.6	0.30	5.9	6.93
		P-ch	-1.89	43.8	-0.35	-13.7	6.96