Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 374-375

Metal Node Contact TFT SRAM Cell for High Speed, Low Voltage Applications

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1. Introduction

The SRAM cell with the design rule below 0.6 μm necessitates the use of polysilicon TFT loads to increase the cell stability [1]. In such cell nodes, the parasitic diode contact is formed through the connection of P^+- to N^+-polysilicon, which degrades the cell operational margin in high speed and low Vcc SRAM products [2].

We fabricated TFTs and TFT SRAM cells with diode and metal node contacts and examined the cell performance. We show that the adverse effect of the diode contact can be fully circumvented by the metal node contact. Also process methodology for incorporating metal node contact is presented.

2. Results, discussion and process methodology

The fabricated bottom gate pTFTs had 0.35/0.7 μm aspect ratio, 0.4 μm drain offset and 270 Å thick channel polysilicon, phosphorus doped at $1.9\times10^{18}/cm^3$. The drain offset and source/drain regions were boron doped at $3.7\times10^{18}/cm^3$ and $1.1\times10^{20}/cm^3$, respectively. The HTO gate oxide was 250 Å. Figure 1 shows the diode and metal contact TFTs, both made by placing 0.45x0.45 μm^2 node and metal contacts in the drain side of TFTs. In metal contact, the aluminum interconnects the P^+ and N^+ polysilicon, eliminating N^+- P^+ diode contact. The measured I-V curves from the two contacts, and the ON current from metal contact TFT are shown. Apparently the low diode contact current limits the TFT ON current for the drain voltage, Vds, below 2.0 V. Thus for Vds below 1.3 V, or equivalently the high node voltage (V_H) over 2.0 V just after write operation, the diode contact severely limits the high node charging current. In contrast, the metal contact current is much larger than TFT ON current, indicating charging is not limited by the contact.

Figure 2 presents the transfer curves from diode and metal contact TFTs for Vds of -0.1 V and 3.3 V. The current reduction at small Vds and the transfer curve shift due to the series resistance appended by the diode contact is apparent.

Figure 3 shows the transfer characteristics from the two cell inverters having the same lateral and horizontal dimensions but different node contacts. The output node voltage, Vout, of the metal contact TFT inverter fully rises to Vcc but for the case of diode contact, Vout rises only to 0.1~0.2 V below Vcc due to the leakage current-induced voltage drop across the diode.

Figure 4 is the simulated Vout of the two inverters versus time when input flips from 3.3 V to 0 V. For simulation, TFT I-V curves were curve fitted. Note that Vout rises to Vcc-0.1 V within 0.09 ms for metal contact inverter, while it takes about 0.65 ms for diode contact inverter.

Figure 5 shows the measured V_H just after write operation, V_{HI}, and simulated high node charging time, t_{ch}, from V_{HI} to Vcc-0.1 V versus Vcc. Since V_{HI} decreases below Vcc/2 for Vcc lower than 2 V, the lower limit of Vcc for stable data retention is 2 V. Note that t_{ch} of the metal contact cell is about 7 times shorter than the diode contact cell, indicating improved cell stability of data retention and low Vcc margin.

Figure 6(a),(b) show I-V curves of the two contacts measured from different locations within the wafer. The large observed non-uniform performance of the diode contact should contribute significantly to the non-uniform performance of the inverter or the cell.

The conventional diode contact process has two critical drawbacks; (a) diode contact formation and (b) gate oxide quality degradation during node contact opening performed on top of the TFT gate oxide. These drawbacks can be avoided by the metal node contact made down to N^+ poly 3 through BPSG, load oxide, P^+ poly 4, TFT gate oxide, as shown in Fig. 7. The cumulative 50 % failure of the constant current stress test for the metal node contact process is improved by 7 times for applied current density of 6.5 mA/cm².

The metal node contact can be incorporated in cell array by plugging the node contact using selective refractory metal, instead of metal 1 in Fig. 7, as shown by the cell layout and cross-section (X-X') in Fig.8. The first cross-section shows the process completed up to poly 3 gate patterning and second one shows the deposition and patterning process of TFT gate oxide, poly 4 channel and load oxide. The third cross-section shows the node contact (X_1-X_2) and refractory metal plugging. The last one shows the completed process.

3. Conclusions

The diode contact severely limits the charging current as V_H is raised to near Vcc and is responsible for the maximum V_H to reach only 0.1~0.2 V below Vcc. The typical charging time is 0.65 ms, and the diode contact adds significantly to non-uniform cell performance. The metal node contact improves the cell performance, including the uniformity. Also, V_H rises fully to Vcc and high node charging time is faster by more than 7 times. The metal node contact can be implemented without additional masks, cell area and gate oxide degradation and the process methodology will be useful for high speed, low power SRAM fabrication.

References

1)S. Ikeda, et al. : IEDM tech. Dig. (1990) p.469.
2)T.F. McNelly, et al. : IEDM tech. Dig. (1995) p.927.

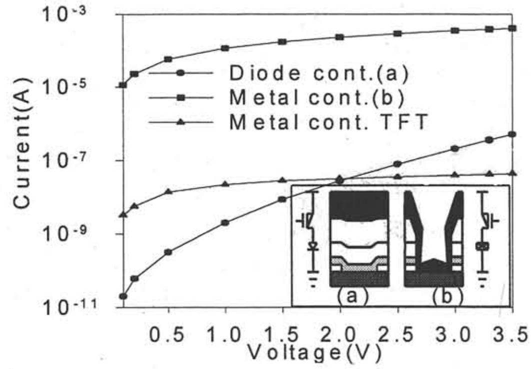

Fig.1 I-V curves from diode(a) and metal(b) contacts (shown in box) and TFT ON current vs. Drain voltage magnitude. The layers in the cross-section are aluminum, BPSG, load oxide, P^+ poly, TFT gate oxide, N^+ poly from the top.

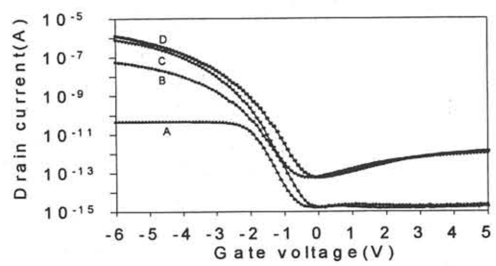

Fig.2 Transfer curves from diode (A,C) and metal (B,D) contact TFTs for drain voltage of -0.1 V (A,B) and -3.3 V (C,D)

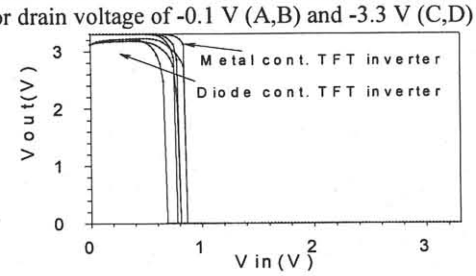

Fig.3 Voltage transfer characteristics from both cell inverters measured from different locations of the wafers

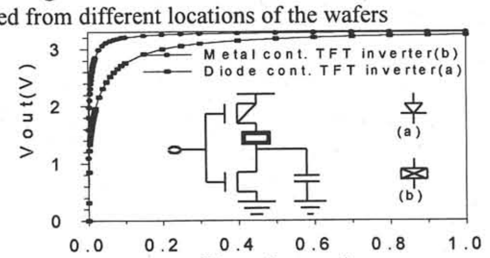

Fig.4 Simulated output node voltage of the diode and metal node contact TFT inverters vs. Time (Vcc=3.3 V, C=15fF)

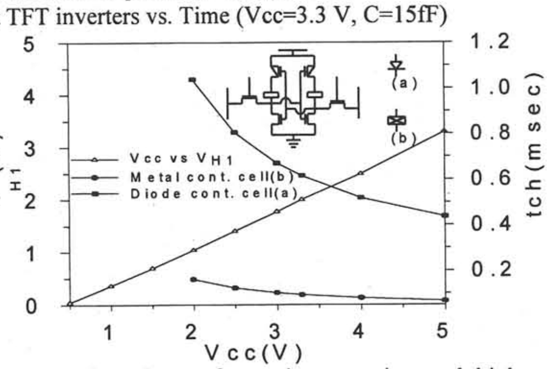

Fig.5 High node voltage after write operation and high node charging time vs. Vcc

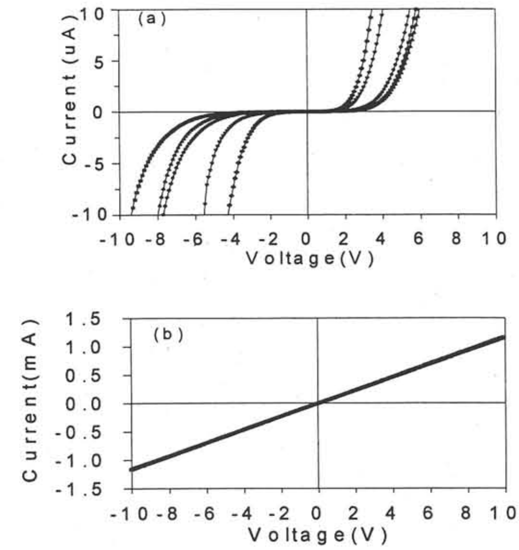

Fig.6 Diode (a) and metal (b) contact I-V curves measured from different locations of the wafer

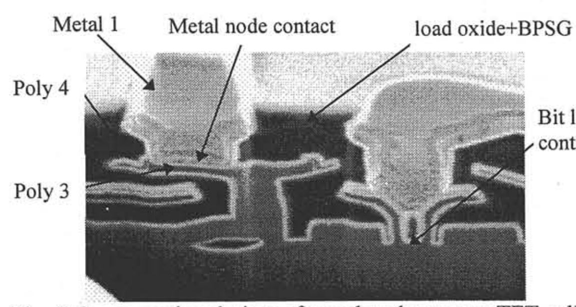

Fig. 7 Cross-sectional view of metal node contact TFT cell

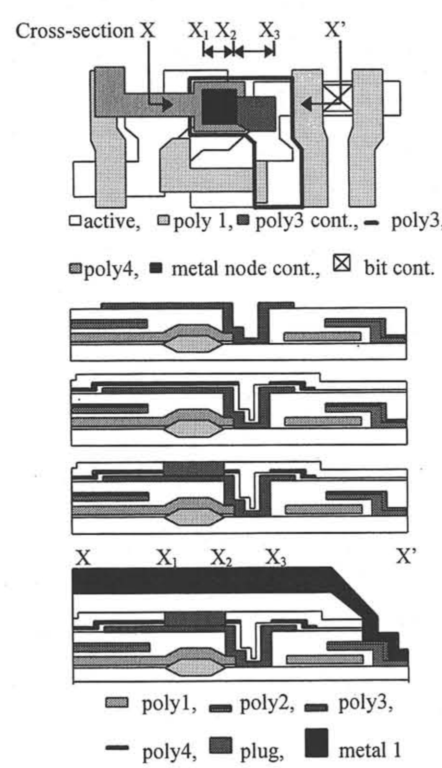

Fig.8 Layout and cross-sectional view of the proposed metal node contact cell