Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 64-65

Improvement in the Electrical Properties of GaAs/InAs/GaAs Structures through the Use of (111)A Substrates

Hiroshi Yamaguchi and Yoshiro Hirayama

NTT Basic Research Laboratories, Morinosato Wakamiya, Atsugi-shi, Kanagawa 243-01, Japan
Phone: +81-462-40-3475, Fax: +81-462-40-4727, E-mail: hiroshi@will.brl.ntt.co.jp

1. Introduction

Heteroepitaxial InAs/GaAs and InAs/AlGaAs systems show good promise for device applications because of their large conduction band discontinuity and the unique electrical properties of InAs, i.e. high activation in n-type doping and Fermi-level pinning in the conduction band [1-3]. Despite this promise, the ability to obtain high quality epitaxial growth in such highly mismatched ($\Delta a_0 \sim 7.2\%$) compound semiconductors systems is hindered by the formation of three-dimensional islands, at least for growth on conventionally used (001) oriented substrates [4,5].

The use of non-(001) surfaces was recently proposed as a means of solving this difficulty. It has been demonstrated that two-dimensional growth of InAs can be achieved on GaAs substrates by using (110) and (111)A surfaces [6,7] since strain can be relaxed on such surfaces with no transformation of the growth mode from layer-by-layer into Stranski-Krastanov mode. We applied this novel technique to fabricate atomically controlled heterostructures in InAs/GaAs systems. In this paper, we report the electrical properties of very thin InAs films embedded between GaAs layers grown on (001) and (111)A substrates. We found that the InAs/GaAs and GaAs/InAs interfaces are both atomically flat, and that the Hall mobility is greatly improved when using (111)A substrates. The results of self-consistent calculations are also given to explain the dependence of carrier concentration on well thickness.

2. Results and Discussions

Undoped InAs layers of various thickness were grown on GaAs (111)A and (001) semi-insulating substrates and then covered by 100nm-thick GaAs films, after 200nm-thick GaAs buffer layers had been grown using solid source molecular beam epitaxy. Figure 1 shows the sheet carrier concentration and the mobility of undoped InAs thin films obtained from standard Hall measurements at room temperature as a function of InAs thickness. All the films show n-type carrier conduction indicating the presence of donor type impurities or defects. The sheet carrier concentration saturates at the level of $3\times10^{12}\mathrm{cm}^{-2}$ for the InAs films thicker than 50nm for both substrates, indicating that the donors are located at the interfaces. If the donor impurities/defects are incorporated/created in the InAs films, the carrier concentration must be proportional to the InAs thickness. This constant sheet carrier concentration was also reported for uncovered InAs films grown on (001) GaAs substrates [1], where both the surface states and interface states can be the source of electrons. We measured similar concentration in our embedded InAs films, and therefore consider the interface states to be the sources of electrons.

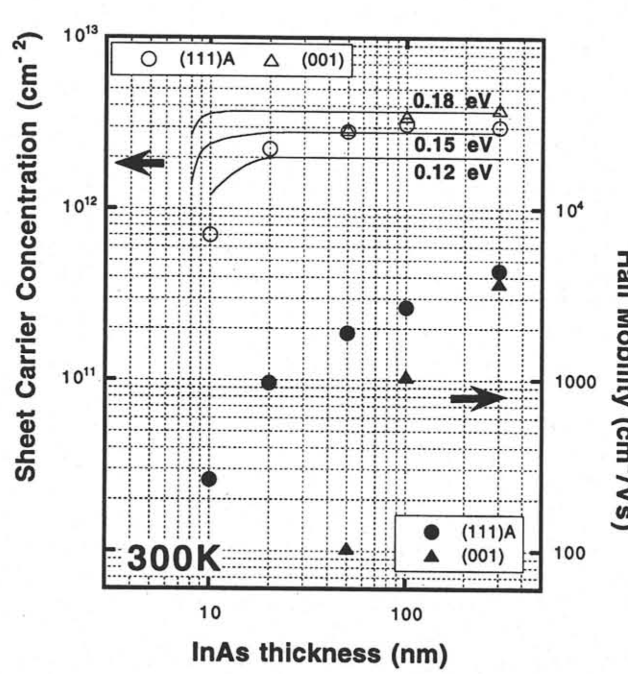

Fig.1 Sheet carrier concentration (open markers) and Hall mobility (closed markers) of InAs films as a function of film thickness for (111)A (circles) and (001) (triangles). Solid lines indicate the concentration obtained from self-consistent calculations assuming interface Fermi level pinning at 0.12 eV, 0.15, and 0.18 eV above CBM.

For (001) substrates, it was found that the mobility was significantly decreases with reduced InAs thickness. It is well known that when InAs films are grown on such substrates, three-dimensional islands are formed via the Stranski-Krastanov mechanism [4,5]. It is our belief that these degrade the flatness of the GaAs/InAs interfaces and that the interface scattering is greatly enhanced as a result. The problem was especially apparent when InAs films thinner than 50nm were used. These films were found to be so highly resistive that Hall measurements could hardly be applied to them. Thick InAs film growth to improve the GaAs/InAs interface flatness is necessary to recover the mobility. In contrast, the Hall mobility under reduced InAs thickness was found to be much higher for the (111)A samples than the (001) samples. This is particularly true for InAs films thinner than 100nm, and an improvement of more than one order of magnitude was observed in 50nm samples. This is because the InAs films grow in a two-dimensional manner on a (111)A substrate and atomically flat GaAs/InAs interfaces are established as a consequence. Even with a 10nm sample, distinct conduction was confirmed for (111)A, although the sheet carrier concentration was reduced.

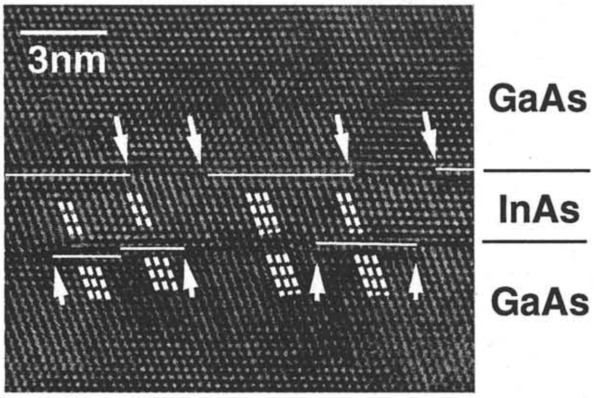

Fig.2 Cross-sectional TEM image of a GaAs/InAs/GaAs structure grown on a (111)A substrate. Arrows and solid lines display the positions of partial dislocations and stacking faults at the interfaces, respectively. Dotted lines are guide to the eye to see the phase shift in the atomic rows.

Figure 2 shows a cross-sectional transmission electron microscopy (TEM) image of a GaAs/InAs/GaAs structure grown on a (111)A substrate. The InAs thickness is only 3nm. In this structure, stacking faults with a period of about 10nm can be clearly seen at the designed positions of both GaAs/InAs and InAs/GaAs interfaces. This observation is consistent with a model for a dislocation network at InAs/GaAs interfaces which has been proposed as a result of STM observation [7]. The present TEM observation clarifies that a network is formed at both the GaAs/InAs and InAs/GaAs interfaces, and that both interfaces are atomically flat. A similar observation of a (001) sample showed that three-dimensional InAs clusters has been formed via the Stranski-Krastanov growth mechanism, and that neither interface was atomically flat.

This observation leads us to believe that high-density dangling bonds related to the dislocation network are localized at the interfaces, and that they act as donor states to pin the Fermi level at the level of the dangling bond states. The pinning position is expected to be in the conduction band because the charge neutrality level (CNL) of InAs has been predicted to be 0.1 eV~0.2 eV above the conduction band minimum (CBM) [8,9]. The carrier saturation after 50nm and reduced carrier concentration before 10nm can be well explained by this Fermi level pinning at the InAs/GaAs and GaAs/InAs interfaces. When the well thickness is reduced, the lowest quantum level rises and approaches the pinned level, leading to the reduced electron concentration. To confirm this more quantitatively, we performed self-consistent calculations assuming the interface Fermi level pinning, and obtained good agreement with the experimental results (see the solid lines in Fig.1). The saturation concentration of $3\times10^{12}cm^{-2}$ gives the position of the interface Fermi level in the range of 0.12-0.18 eV. This value is close to the reported position of surface Fermi level pinning [2,3] and the CNL of InAs [8,9].

3. Conclusion

We have compared the electrical properties of InAs thin films embedded in GaAs layers on (111)A and (001) substrates. Major improvement in Hall mobility through the use of a (111)A substrate was confirmed, specially for a structure having InAs films thinner than 300nm. The carrier concentration was found to saturate at a value of $3\times10^{12}cm^{-2}$ after the InAs thickness reached 50 nm. Self-consistent calculation assuming interface Fermi level pinning produced results showing good agreement with the experimental results, and the Fermi level position was estimated to be in the range of 0.12-0.18 eV.

References

1). A.A. Kubiak, E.H. Parker, S. Newstead, and J.J. Harris, Appl. Phys. A **35**, 61 (1984).

2). C.A. Mead and W.G. Spitzer, Phys. Rev. **134**, A713 (1964); J.N. Walpole and K.W. Nill, J. Appl. Phys. **42**, 5609 (1971).

3). P.D. Wang, S.N. Holmes, T. Lee, R.A. Stradling, I.T. Ferguson, and A.G. de Oliveira, Semicond. Sci. Technol. **7**, 767 (1992).

4). M. Yano, M. Nogami, Y. Matsushima, and M. Kimata, Jpn. J. Appl. Phys. **16**, 2131 (1977).

5). B.T. Meggit, E.H.C. Parker, and R.M. King, Appl. Phys. Lett. **33**, 528 (1978).

6). X.M. Zhang, D.W. Pashley, J.H. Neave, J. Zhang, and B.A. Joyce, J. Cryst. Growth **121**, 81 (1992); J.G. Belk, J.L. Sudijono, X.M. Zhang, J.H. Neave, T.S. Jones, and B.A. Joyce, Phys. Rev. Lett. **78**, 475 (1997).

7). H. Yamaguchi, M.R. Fahy, and B.A. Joyce, Appl. Phys. Lett. **69**, 776 (1996); H. Yamaguchi, J.G. Belk, X.M. Zhang, J.L. Sudijono, M.R. Fahy, T.S. Jones, D.W. Pashley, and B.A. Joyce, Phys. Rev. **B55**, 1337 (1997).

8). V. Heine, Phys. Rev. **A138**, 1689 (1965).

9). J. Tersoff, Phys. Rev. Lett. **52**, 465 (1984); Phys. Rev. **B32**, 6968 (1985).