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Invited

Ultrahigh-Speed Integrated Circuits Using InP-Based High-Electron-Mobility Transistors(HEMTs)

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1. Introduction

Recently developments in optical communications technology already enable the commercial use of 10-Gbit/s systems. Experimental development of the next generation of cost-effective TDM and WDM optical fiber networks has started [1, 2]. It is very important for device researchers to clarify and demonstrate how fast ICs can operate.

InAlAs/InGaAs HEMTs have achieved record current gain cutoff frequency (f_T), transconductance (g_m) , and maximum oscillation frequency (f_{max}) and are considered to be the fastest devices at room temperature. An f_T and f_{max} of over 200 GHz and a g_m of over 1000 mS/mm are available using 0.1-μm-gate devices in ICs [3]. In addition to demonstrating the feasibility of the device for MMICs, we have successfully expanded the applicable field of the device to high-speed digital ICs by introducing an InP recess-etch stopper [4] and by monolithically integrating a vertical diode as a level-shifter [5]. In this paper, we discuss to what extent HEMTs can meet the requirements for ultrahigh-speed digital ICs and over 40-Gbit/s ICs and modules, which we have achieved so far, are summarized.

2. Device Design and Performance

Figure 1 summarizes g_m and f_T of III-V FETs ever reported. It can be reasonably considered that the increase in g_m corresponds to the vertical scaling (thinning a barrier thickness, d) and that the increase in f_T corresponds to the lateral scaling (shortening a gate length, L_g). Both f_T and g_m for InAlAs/InGaAs HEMTs are remarkably higher than those for others. This advantage results from the better electron transport properties, the low parasitic resistance, and the scale-down of the channel. In the graph, gate-delay-time (τ_{pd}) contours calculated using an analytical expression for the τ_{pd} of SCFL (Source Coupled FET Logic) [6] are also shown. Other parameters assumed in the calculation were those extracted from our fabricated InAlAs/InGaAs HEMTs. The contours clearly shows that it is important to achieve an effective balance between g_m and f_T for high speed operation. The-state-of-the-art performance of InAlAs/InGaAs HEMT (f_T=200 GHz, g_m=1.2 S/mm) should result in an intrinsic τ_{pd} of about 4 ps/gate which is small enough for achieving over 40 Gbit/s operation even if we take the transmission delay into account [7]. Reproducibility and uniformity of the device performance are crucial to achieve such high-speed digital ICs.

Figure 2 shows the structure of our HEMT with an InP recess-etch stopper. The layers were grown by MOCVD. The InP recess-etch stopper enables us to design the barrier thickness precisely and reduces the threshold voltage scattering. To keep the g_m of over 1 S/mm, the total barrier thickness including the 50-Å-thick InP layer was designed to be 140 Å. The sheet density of the δ-doping was designed so that the threshold voltage (V_{th}) was -0.5 V. To get abrupt

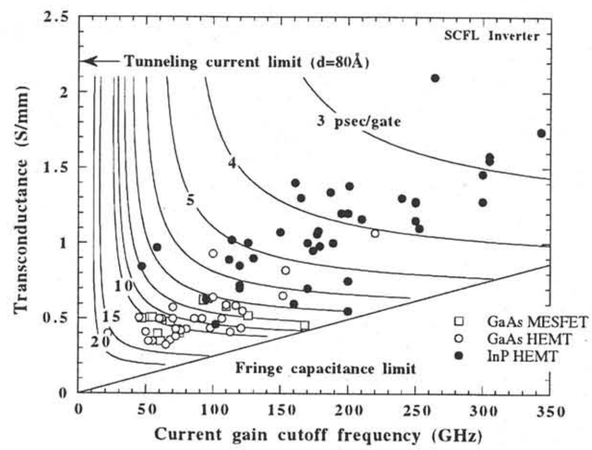

Figure 1. gm and fT of various FETs and gate delay contours of an SCFL inverter.

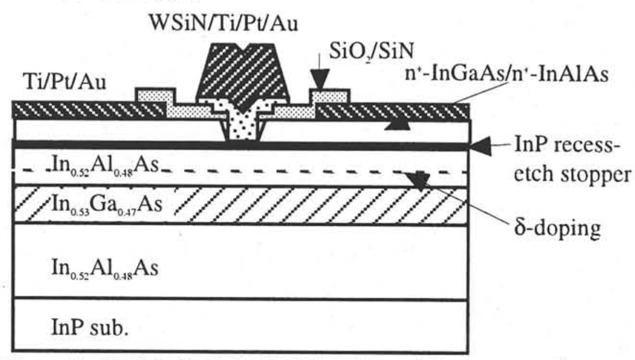

Figure 2. InAlAs/InGaAs HEMT with an InP recess-etch stopper.

Table I. Example of Performance for 0.1-μm-gate InAlAs/InGaAs HEMTs on a 2-inch wafer (N=32)

	Average	Standard deviation
V_{th} (mV)	-419	32
g_m (S/mm)	0.95	0.032
f_T (GHz)	174	7.2
f_{max} (GHz)	~523	43

heterointerfaces between InP and InAlAs, growth conditions for the materials and gas-switching sequences have been optimized. Ohmic contacts are formed by the non-alloyed metals with the n+-InGaAs/n+-InAlAs cap layers. The contact resistance was 0.07 •mm. WSiN is used as a Schottky metal for the InP layer for the better thermal stability comparing with Ti [8].

Table I summarizes an examples of performance for 0.1-μm-gate InAlAs/InGaAs HEMTs on a 2-inch wafer. Although the g_m is lower than our expectation as a penalty of the lateral etching during the gate-recess etching, the value still retain 0.95 S/mm and C_{gd} decreases by a factor of 2. The small feed-back capacitance increases f_{max} and is also advantageous for high-speed operation of SCFL circuits.

In addition to FETs, a level-shift diode is also needed in digital ICs. To reduce the interconnection length and CR-delay time, a small diode with a low turn-on resistance is required. For this purpose, InGaAs-pn layers [4] or InAlAs-Schottky layers were grown on the HEMT layers with an n^+-InP etch stopper. One-level and cross-over interconnection lines were made by a lift-off and an electro-plating methods, respectively. MIM capacitors were made with a SiN film

3. Over 40-Gbit/s ICs

Table II summarizes IC sets using our InAlAs/InGaAs HEMTs for 40 Gbit/s optical transmission experiments. To boost the operation bit rate of ICs and modules as high as possible, the following novel circuit technologies were used.

(1) Distributed-circuit design techniques [9,10,11].
(2) High-speed Latching Operation Flip-Flop circuit [12]
(3) Super-Dynamic Flip-Flop circuit [13].
(4) Wideband data and clock buffer using peaking and feedback techniques [14]
(5) Chip-size cavity package with 6-RF ports [15]

The highest operation bit rate of 64 and over 40 Gbit/s for multiplexers (MUX) and demultiplexers (DEMUX) were measured on wafer. Error-free operations up to the maximum bit rates were confirmed. The packaged IC modules for the MUX and DEMUX also operated at beyond 40 Gbit/s. Electrically multiplexed and demultiplexed 40 Gbit/s, 300-km transmission has been successfully demonstrated using the IC modules described above [14, 16].

4. Prospect

As shown in Fig. 1, increase in g_m is more effective to reduce the gate delay than an increase in f_T is. Reducing source resistance and thinning the barrier are more crucial. Minimum barrier thickness limited by the tunneling current was estimated to be 80 Å [17] and intrinsic g_m of 2.2 S/mm is estimated for the barrier by assuming the saturation velocity of 2.7×10^7 cm/s. f_T of over 250 GHz and g_m of 1.5 S/mm have been demonstrated by a few groups using InP-based HEMTs. 3 ps/gate operations, which is small enough for 80 Gbit/s ICs, is becoming realistic after improving uniformity and reproducibility.

5. Conclusions

A 0.1-µm-gate InAlAs/InGaAs HEMT with an f_T of over 160 GHz and a g_m of 1 S/mm is now available for application in circuits. An InP recess-etch stopper improved the uniformity of threshold voltage and enabled us to apply the HEMTs in digital ICs. Novel circuit technologies make the most of the high-speed performance of the devices and boost the operating speed of ICs. As a benchmark for future large-capacity networks, electrically multiplexed and demultiplexed 40 Gbit/s, 300-km transmission was successfully demonstrated using InP-based HEMT ICs. Although there are remaining issues which should be solved in their practical use, there is a wide room for increasing the operation speed of ICs using InP-based HEMTs.

Table II Summary of ICs and modules for optical transmission experiments using InAlAs/InGaAs HEMTs.

Circuit	Bandwidth/ Bit rate	Gain (dB)	Output	Power (W)
2:1 MUX[14]	1-64 Gbit/s (1-52 Gbit/s)*	----	0.92V_{pp}	2.2
Preamp. [10]	DC-32 GHz	9	1.0V_{pp}	0.44
Baseband amp.[9]	DC-47 GHz	16	1.2V_{pp}	1.1
Signal distributor [11]	DC-100 GHz	-2.5	0.5V_{pp}	1.1
Decision [14]	15->40 Gbit/s (15-46Gbit/s)*	---	0.94V_{pp}	1.7
1:2 DEMUX [14]	2-40 Gbit/s (2-40 Gbit/s)*	---	0.94V_{pp}	3.8
Frequency Divider[4]	DC-40.4 GHz	---	0.4V_{pp}	0.55
Frequency Divider[14]	2-46 GHz	---	0.9V_{pp}	1.1
Limiting amp. [10]	34-40 GHz	17	10dBm	0.070

*:Performance of packaged IC modules

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