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Novel Gate-Recess Process for the Reduction of Parasitic Phenomena Due to Side-Etching in InAlAs/InGaAs HEMTs

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1. Introduction

InP-based InAlAs/InGaAs high-electron-mobility transistors (HEMTs) have demonstrated excellent high-frequency characteristics and have a potential to achieve a cutoff frequency (f_T) of over 300 GHz by reducing the gate length (L_g) and barrier thickness. As L_g becomes shorter, the extent of an etching front in a lateral direction that is side-etching, which accompanies the wet-chemical etching commonly used for gate-recess etching has a greater effect on device performance. When the electron density in the side-etched region is small, the extent of the side-etching causes the increase in a parasitic source resistance and in its related phenomena such as kink[1]. Futhermore, the extent of metal front to the side-etched region and the extent of electric force line from the gate-metal edge to the side-etched region make the effective gate length longer than the patterned gate length, resulting in device performance lower than estimated. We therefore studied a gate-recess process for keeping the electron density in the side-etched region high using a *two-step recess* etching in which a dry etching is combined with a conventional wet-chemical etching and InP-etching-stopper-layer technology[2]. The resulting structure is similar to a buried-gate structure with good uniformity and reproducibility. For the selective dry etching, Ar plasma etching is used. We found that Ar plasma etching with low power provides an etching rate for InAlAs which is quite low compared with the etching rate of InP[3].

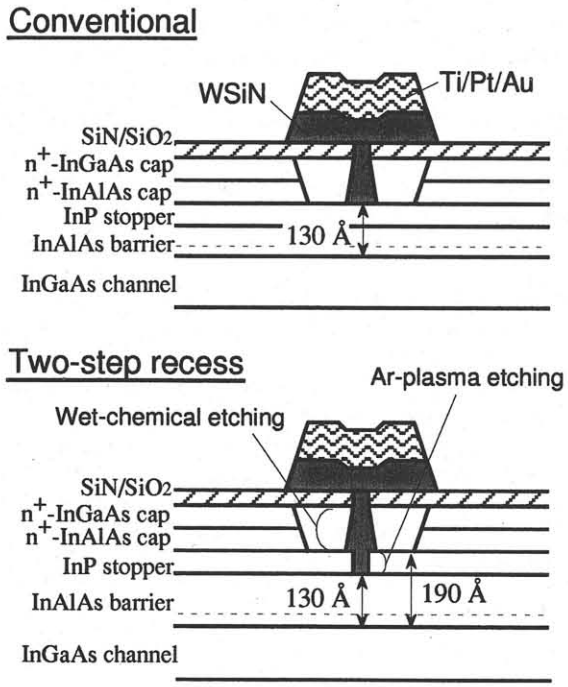

Fig. 1. Schematic cross section of gate structure of conventional and *two-step recess* process. In two-step recess process, InP stopper layer is removed by Ar-plasma dry etching to avoid side-etching.

2. Device structure and fabrication

Materials were grown on (100) InP substrates by metal organic chemical vapor deposition (MOCVD). The epitaxial layers consisted of i-InAlAs buffer (2000 Å), i-InGaAs channel (150 Å), iInAlAs spacer (30 Å), carrier supply (δ-doped), i-InAlAs barrier, i-InP etching stopper, n+-InAlAs cap (200 Å), and n+-InGaAs cap (200 Å). Figure 1 shows the schematic cross section of the gate structure. In making the conventional structure only the wet-chemical etching is performed and the gate metal is on the InP etching-stopper layer. In the two-step recess structure the first etching is performed by wet-chemical etching down to the InP stopper, and then the dry etching removes the InP stopper layer and the gate metal makes direct contact with the InAlAs barrier layer. Both structures have the same distance between the gate metal and channel layer to equalize the threshold voltage (V_{th}) and intrinsic part of the transconductance (g_m). Barrier thickness in the side-etched region of the two-step recess structure, however, is greater than that of the conventional structure. This is an advantage of the two-step structure because a thicker barrier results in a higher electron density in the side-etched region. Since the second etching should remove only the InP layer and should leave the InP stopper layer in the side-etched region, a selective dry etching is required. The conventional technologies of the selective etching of InP over InAlAs, however, is reactive ion etching (RIE) using fluorine (F) containing gas to gain the selectivity[4]. This may be inappropriate for the gate-recess process because residual F atoms may diffuse into Si-doped InAlAs and cause the degradation of the carrier density of the

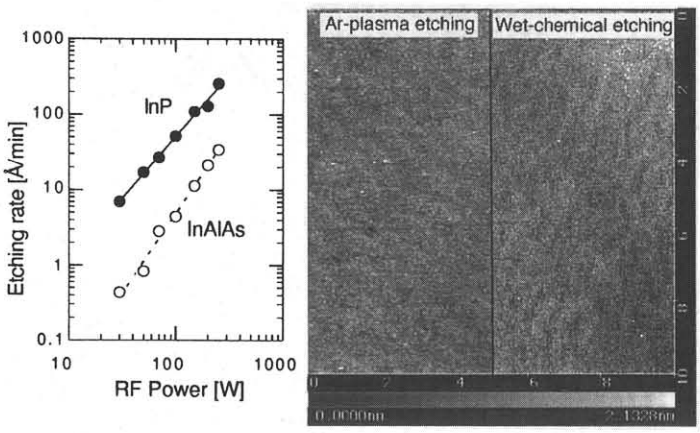

Fig. 2. (Left) RF power dependence of etching rate by Ar-plasma etching. (Right) AFM image (10 x 10 μm) of the surface of an InAlAs structure after the InP stopper layer is removed by Ar-plasma etching and wet-chemical etching. Ar-plasma etching was performed at an power of 50 W (self-bias voltage: 26 V), Ar flow of 80 sccm, and chamber pressure of 1 Pa. Steps of InAlAs atomic layers are clearly observed even after Ar-plasma etching.

Table I. Mean value and standard deviation (σ) of threshold voltage (V_{th}) and transconductance (g_m) of 64 HEMTs on a 2-inch wafer. L_g = 0.12 μm.

		Conventional	Two-step recess
$<V_{th}>$	[V]	**-0.227**	**-0.233**
σ_{Vth}	[V]	0.028	0.048
$<g_m>$	[S/mm]	**0.97**	**1.20**
σ_{gm}	[S/mm]	0.081	0.037

HEMTs[5]. We found instead that Ar plasma etching provides the selectivity. At a RF power of 50 W (0.1 W/cm²), the etching rates of InP and InAlAs are about 17 and 1 Å/min as shown in Fig. 2. Corresponding self-bias voltage of the wafer stage is 26 V, which is much smaller than that in the reported RIE process and may be effective for the reduction of plasma-induced damages. The atomic force microscope (AFM) images of two samples with their InP stopper layers removed by Ar-plasma etching (left) and wet-chemical etching (right) are compared in Fig. 2. The morphology of the Ar-plasma etched surface is as good as the one of the wet-chemical etched surface.

3. Device performance

Table I shows the mean value and standard deviation of V_{th} and g_m of 0.1-μm-gate HEMTs on a 2-inch wafer. The two-step recess etching yields good uniformity comparable to the conventional process due to the selectivity of Ar-plasma etching. Note that g_m of the two-step recess structure is about 20 % higher than the conventional structure in spite of same barrier thickness and similar V_{th}. Moreover, the standard deviation of g_m is reduced by a factor of 2 by using the two-step recess process. Figure 3 shows the gate-to-source voltage (V_{gs}) dependence of f_T. The two-step recess structure provides higher f_T and the difference of f_T becomes larger as the V_{gs} increases. These results show that the source resistance due to the side etching has been considerably reduced by using the two-step recess technology. As V_{th} becomes higher, the electron density of the side-etched region decreases in the conventional structure. Thus the advantage of the two-step recess structure will be observed clearer as V_{th} becomes higher. Figure 4 shows the correlation between L_g and f_T. In the conventional structure, f_T becomes saturated and the difference of f_T between the two structures becomes larger as L_g becomes shorter. This result suggests that the two-step recess structure can also reduce the extent of the effective gate length.

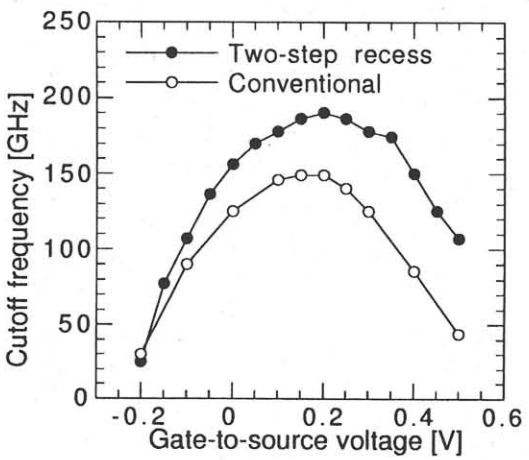

Fig. 3. Correlation between gate-to-source voltage (V_{gs}) and cutoff frequency (f_T). Drain-to-source voltage (V_{ds}) is 1.0 V. L_g = 0.12 μm.

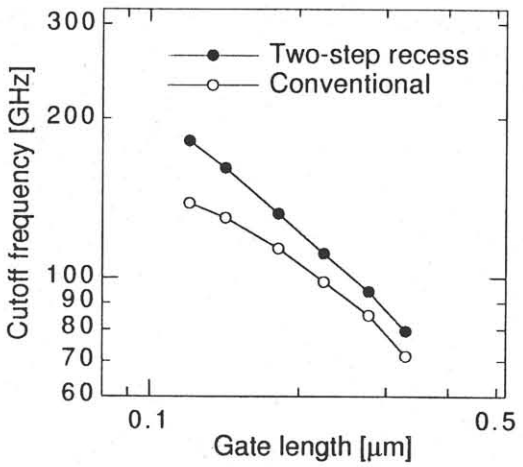

Fig. 4 . Correlation between gate length (L_g) and maximum value of cutoff frequency (f_T). V_{gs} = 0.2 V, and V_{ds} = 1.0 V. Gate patterns replicated on SiN/SiO_2 were measured as L_g's values.

4. Conclusions

A novel gate-recess technology provided by the two-step recess etching, the sequence of wet-chemical etching down to the InP stopper layer and Ar-plasma etching to remove the stopper layer, was studied. The Ar-plasma etching could remove the InP stopper layer without considerable side-etching. By leaving the InP stopper layer in the side-etched region, the electron density of the region can be kept high, resulting in the reduction in the source resistance and the effective gate length. This technology is effective for 0.1- and sub-0.1-μm-gate HEMTs.

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References

[1] T. Suemitsu, T. Enoki, M. Tomizawa, N. Shigekawa, and Y. Ishii, Proc. 9th Int. Conf. InP and Related Materials (Hyannis, MA, USA, 1997), p. 365.

[2] T. Enoki, H. Itoh, K. Ikuta, and Y. Ishii, Proc. 7th Int. Conf. InP and Related Materials (Sapporo, Japan, 1995), p. 81.

[3] T. Suemitsu, T. Enoki, and Y. Ishii, submitted to Appl. Phys. Lett.

[4] for example, S. J. Pearton and W. S. Hobson, Appl. Phys. Lett. **56**, 2186 (1990).

[5] N. Hayafuji, Y. Yamamoto, N. Yoshida, T. Sonoda, S. Takamiya, and S. Mitsui, Appl. Phys. Lett. **66**, 863 (1995).