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High-Performance Recessed Gate HFETs with New Doped Channel Structure

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1.Introduction

Over the past decade, High Electron Mobility Transistors (HEMTs) have become accepted as one of the most important key devices for microwave to millimeter wave applications. Besides HEMTs, however, doped-channel hetero-structure FETs (doped channel HFETs) have also long been considered as another useful candidate for those high frequency applications.

The doped-channel HFETs reported to date in fact have shown such superior characteristics as excellent linearity[1], high breakdown voltage[2], large intrinsic transconductance[3]. Nevertheless, an insulating layer commonly buried under the gate electrode inevitably causes high channel series resistance and seriously degrades the extrinsic transconductance[4]. As a result, the RF characteristics obtained so far are not as good as expected. Many attempts have been made to overcome these problems, but most of them use complicated fabrication process and in turn induce different new problems such as threshold voltage shift and breakdown voltage lowering[5,6].

In this paper, we propose and demonstrate a new doped-channel HFET structure. This new device can solve the above problems, and the fabricated prototypes show RF performance comparable to, or even superior to that of pseudomorphic HEMT (PHEMT) reported to date.

2.Device Structure and Fabrication

A schematic cross-section of the fabricated doped-channel HFET is shown in Fig.1. It consists of a doped GaAs/InGaAs/GaAs quantum well and thick GaAs contact layer grown by Molecular Beam Epitaxy on a S.I. GaAs substrate. The strained 10nm n^+-$In_{0.2}Ga_{0.8}As$ channel is doped to $5x10^{18}cm^{-3}$. The n^+-GaAs contact layer doped at $6x10^{18}cm^{-3}$ is grown to 100nm to reduce series resistance and make a homo-junction with the thin 15nm i-GaAs barrier layer. Due to the n-GaAs/i-GaAs homo-junction structure, a spike-shaped barrier with barrier height of 0.15eV, corresponding to i-GaAs/n-InGaAs conduction band discontinuity, is formed at its interface. Therefore, unlike the conventional HFETs, low access resistance (Rs=0.2ohm-mm) can be achieved despite the existence of insulator between the contact and channel layers. Thickness of the i-GaAs insulating layer is optimized to be 15nm to isolate the gate electrode and also to minimize the series resistance simultaneously. Figure 2 shows a dependence of tunneling current on barrier thickness. The solid line corresponds to the current flowing across the spike barrier under the ohmic region and the dotted line to the current across the gate insulator at the pinch off voltage (Vp=-0.5V). It can be seen that at the insulator thickness of 15nm large tunneling current is obtained under the source and drain region, while the gate is substantially kept isolated. The devices are fabricated by our standard technology. The 0.2um T-gates were defined by i-line lithography with phase shifting mask. The surface is passivated with SiNx.

3.Results and Discussion

Typical Id,Gm-Vg characteristics of 0.2um doped-channel HFETs are shown in Fig.3. Average maximum transconductance is as high as 660mS/mm (Vg=0.2V) with a standard deviation of 41mS/mm across the 3-inch wafer. The average output conductance Gd is measured to be 30mS/mm giving a static gain(Gm/Gd) of 33. Maximum drain current exceeding 400mA/mm at Vg=0.6V and large K-value over 900mS/V/mm at the subthreshold region (Vg=-0.1V) indicate its high current drive capability.

The S-parameters of the devices were measured in the frequency range from 0.5 to 40GHz. Figure 4 shows the calculated current gain H_{21}, maximum stable gain MSG and maximum unilateral power gain Gu. Typical current gain cut off frequency fT of 113GHz and maximum oscillation frequency fmax of 200GHz are obtained by extrapolating the H21 and Gu curve by using -6dB/oct gain roll-off. Noise figure measurements have been carried out on wafer between 2 and 18GHz. The obtained minimum noise figure is typically 0.48dB and the associated gain is 12dB at 12GHz (2V,10mA). To our knowledge, these data are the best of the reported values among 0.2um GaAs FETs including PHEMTs [7]. Equivalent circuit parameter analysis suggests that these excellent RF characteristics are attributed to the relative low gate-source capacitance, low parasitic resistance and high transconductance due to the optimized thin gate insulator.

4. Conclusion

We have proposed a new recessed gate doped channel HFET. This structure consists of insulating thin GaAs barrier layer to reduce an access resistance while keeping the gate isolated. The 0.2um gate doped-channel HFETs demonstrate excellent DC and RF characteristics. These results are attributed to the relative low gate capacitance and parasitic resistance inherent of this new structure. This device expected to be useful for high speed digital and millimeter wave applications.

References

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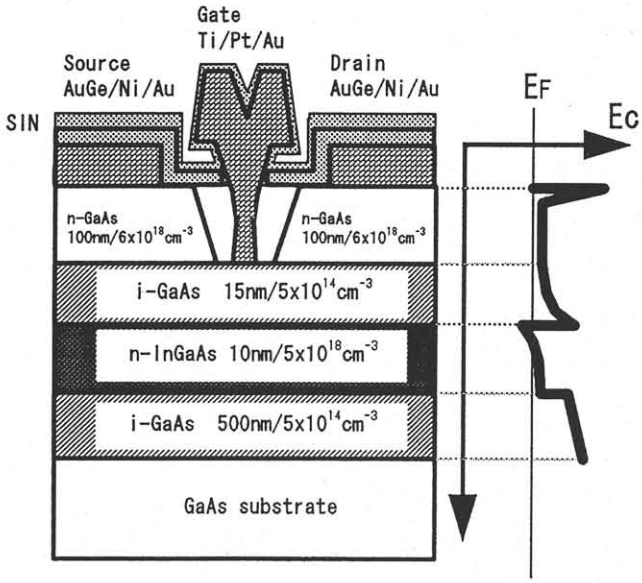

Fig. 1 Cross-section and Energy band diagram of DC-HFET

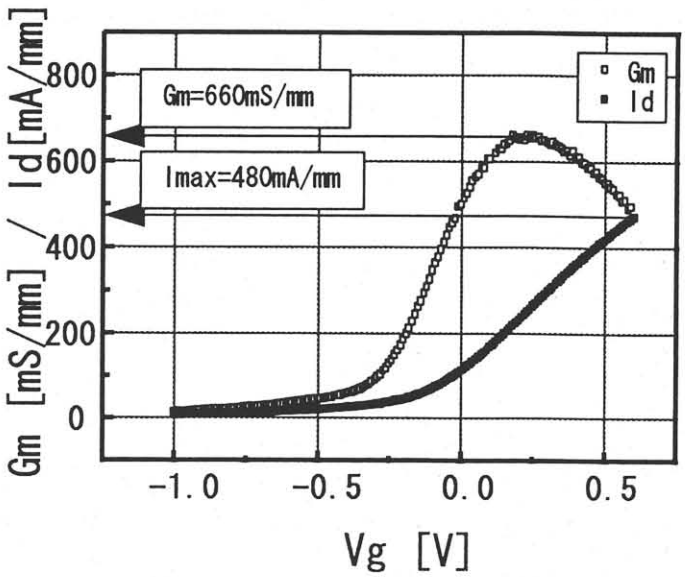

Fig. 3 DC characteristics of 0.2um gate DC-HFET

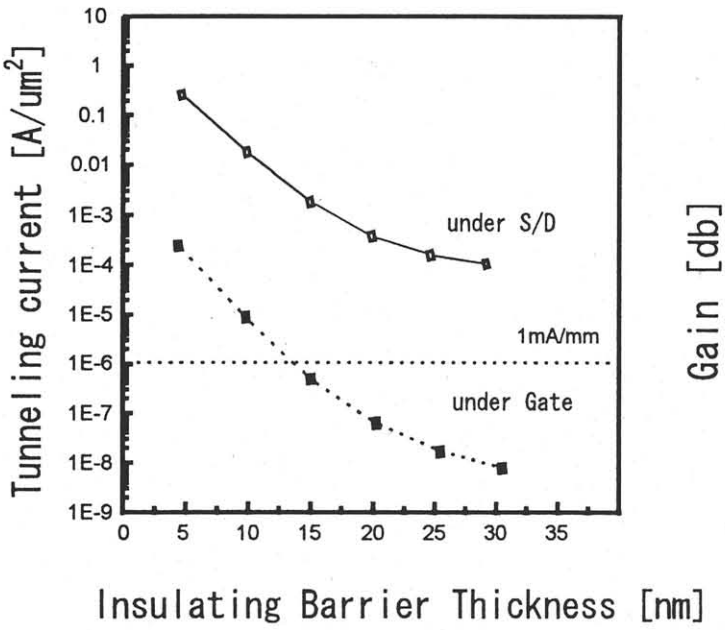

Fig. 2 Dependence of tunneling current on barrier thickness

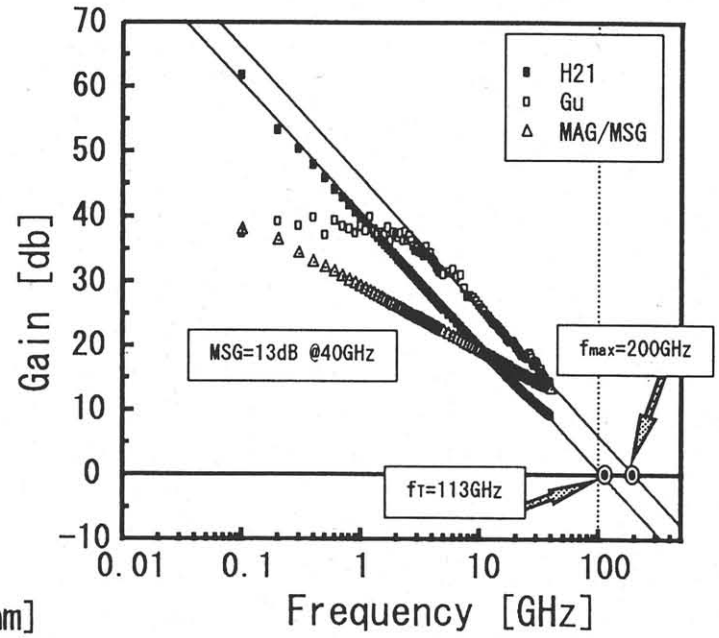

Fig. 4 RF characteristics of 0.2um gate DC-HFET