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High-Speed Static Frequency Divider Employing Resonant Tunneling Diodes and HEMTs

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1. Introduction

Resonant tunneling diodes (RTDs) have been attracting much attention recently due to their ultra-fast switching times [1] and negative differential resistance (NDR) characteristics at room temperature. Two NDR devices, with the capability to modulate the peak current, connected in series can constitute a logic gate known as a monostable-bistable transition logic element, MOBILE [2]. The edge-triggered latching property of the MOBILE helps to simplify the configuration of various logic circuits.

Recently, high-speed operation up to 18 Gbit/s of a MOBILE-based flip-flop circuit was reported [3], and it was shown that the MOBILE has the potential for high-speed and low-power operation as a logic gate. We also proposed a novel circuit configuration for a static frequency divider, featuring reduced circuit complexity by utilizing RTDs in combination with HEMTs, and demonstrated a proper operation at low frequency [4].

This paper reports on a simplified circuit configuration for a static binary frequency divider, employing RTDs and HEMTs, and high-speed operation up to 34 GHz at room temperature.

2. Device Structure

The circuit was fabricated by the InP-based RTD/HEMT integration technology [5]. The epitaxial layers of the RTDs and the HEMTs were grown by MBE. The cross sectional view of the devices is shown in Fig. 1. The HEMT has a 4-nm-thick n^+-InAlAs ($1\times10^{19}cm^{-3}$) carrier supply layer and a 15-nm-thick i-InGaAs channel. The RTD has the double barrier structure of InGaAs (1.2 nm) / InAs (2.8 nm) / InGaAs (1.2 nm) sandwiched by AlAs (1.4 nm) barriers. The electrical characteristics of the devices in a circuit are shown in Fig. 2. The RTDs have a peak voltage of 0.22 V and a peak current density of 8×10^4 A/cm^2, and the HEMTs, with a 0.7-μm gate length, have a cutoff frequency f_T of 38 GHz.

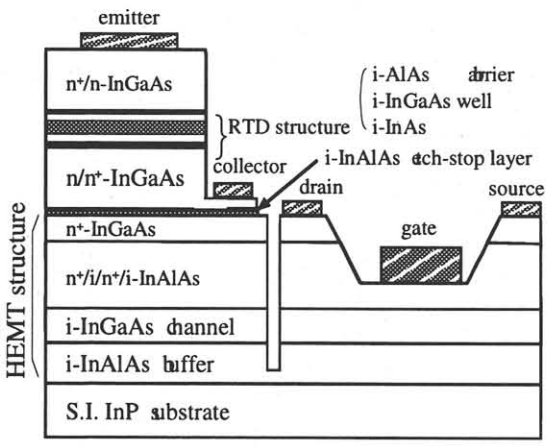

Fig. 1. The cross sectional view of the devices.

3. Circuit Configuration

Figure 3 shows the circuit configuration of the fabricated static binary frequency divider. Its core circuit is composed of only four RTDs and two HEMTs. The number of devices is about one-fifth of that of the conventional SCFL frequency divider. Such simple configuration of the core circuit is due to the NDR characteristics of the RTDs. The core circuit consists of two sub-circuits, each of which contains two RTDs connected in series. The clock signal is directly applied to the serially connected RTDs. The termination resistor, R_T, was loaded at each clock-input node. In the sub-circuit, SC1, a HEMT is connected in parallel to the lower RTD in order to modulate the peak current of this RTD. In the sub-circuit, SC2, the HEMT for modulating the peak current is connected to the upper RTD. In each sub-

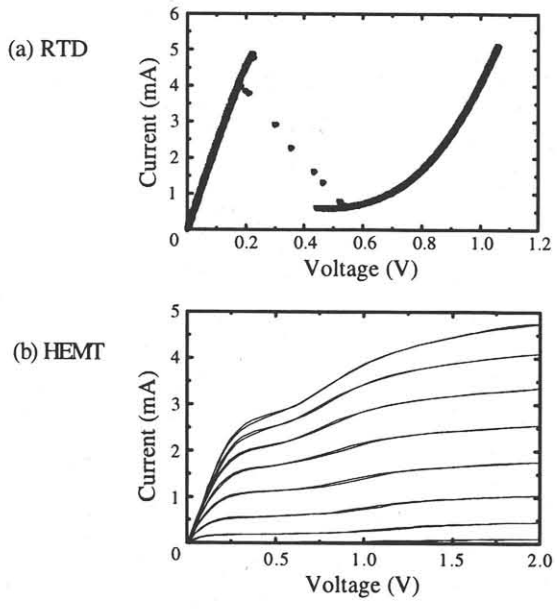

Fig. 2. I-V characteristics of (a) RTD and (b) HEMT at room temperature. (a) The emitter area is 2×3 μm^2. (b) The gate length and width are 0.7 μm and 10 μm, respectively. Gate voltage ranges from -0.2 V to 0.5 V in 0.1-V steps.

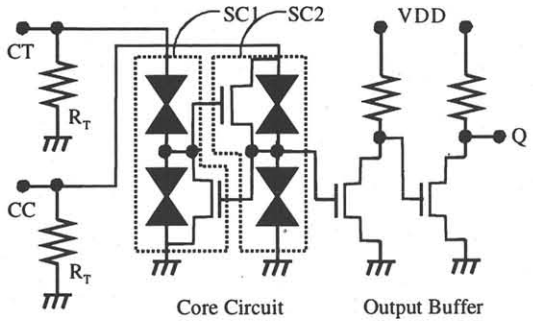

Fig. 3. Circuit configuration of the fabricated static frequency divider.

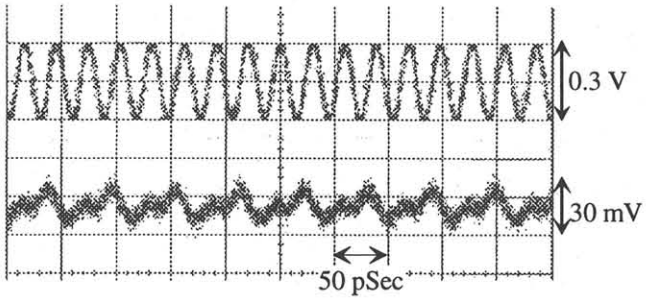

Fig. 4. Input (upper) and output (lower) waveforms of the static frequency divider at 34 GHz.

circuit, we can regard the gate terminal of the HEMT as the input terminal and the node where two RTDs are connected as the output node. In addition, to obtain the proper operation of the circuit, we must make sure of the matching between the logic levels for the inputs and the outputs of the sub-circuits. This is the key point to design such logic circuits as the frequency divider.

The operating principles of the sub-circuits are as follows [2, 4]. First, the output is determined by the difference in the peak current between two RTDs at the rising edge of the applied clock, i.e. if the peak current of the lower RTD is smaller than that of the upper one, the output is high, and vice versa. Second, the sub-circuits keep the output while the clock is high. And third, the sub-circuits are reset at the falling edge of the clock and they are off while the clock is low.

Sub-circuit 1 (SC1) is regarded as the clocked inverter because the emitter area of the upper RTD is designed to be larger than that of the lower one and the HEMT for the input is connected to the lower RTD. On the other hand, SC2 is regarded as the clocked buffer because the emitter area of the upper RTD is designed to be smaller than that of the lower one and the HEMT for the input is connected to the upper RTD. When the input to SC1 is X (X is low or high) at the rising edge of the clock, CT, the output of SC1 is $\overline{X}$ (the complementary signal of X). And SC2 outputs $\overline{X}$ while the clock, CC, is high. When CT becomes high again, the input to SC1 is changed to $\overline{X}$. Namely, the input to SC1 is inverted after one period of the clock. Thus, this circuit works as a frequency divider.

Such operation is possible only under the condition that one sub-circuit can receive the output of the other sub-circuit. Thus, the offset of both clocks is chosen to overlap the on-state of the sub-circuits.

4. Experimental Results

High-speed operation up to 34 GHz was confirmed for the fabricated frequency divider at room temperature. This result is shown in Fig. 4. This frequency is close to the f_T of 38 GHz of the HEMTs in the circuit. The amplitude of the applied clock is 0.3 V. The output signal comes from the output buffer, which consists of two-stage DCFL inverters. The small output swing is due to the interface mismatch between the core circuit and the output buffer. The logic swing in the core circuit is estimated to be as large as 0.5 V.

The experimental high-speed operation clearly shows that input/output level matching in the core circuit has been obtained. This matching ensures the design capability of various logic circuits. Moreover, the power consumption in the core circuit is estimated to be less than 10 mW. Such a small value is due to the reduced number of devices in the circuit and the small capacitance of the RTDs. This low-power consumption is very remarkable for a high-speed logic circuit.

5. Summary

We demonstrated the high-speed operation of a static binary frequency divider employing RTDs and HEMTs. Its operating speed of 34 GHz is almost equal to the f_T of the 0.7-μm gate HEMTs used in the circuit. We also showed the low-power consumption along with the high-speed operation. The circuit configuration was simplified, compared to the conventional SCFL circuits, because of the NDR characteristics of the RTDs. Furthermore, it provides the high-speed operation and low power consumption.

The presented result promises that a circuit employing RTDs and HEMTs will be highly competent for the construction of ultra-high-speed and low-power logic circuits.

Acknowledgments

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