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Effects of Segregated Ge on Electrical Properties of SiO_2/SiGe Interface

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1. Introduction

A pileup of Ge resulted in a degraded oxide/semiconductor interface properties and lower break-down voltages. Shifts on the threshold voltage and the interface state density $>10^{12}/cm^2eV$ were observed on a wet oxidized SiGe layer [1]. In opposite to an oxide grown on a pure Si, the fixed oxide charges were negatively charged. Much attempt to reduce the fixed oxide density and the interface state density has been given by using H_2, N_2, and H_2O annealings [2-4] and by using PECVD grown oxides [5]. For PECVD oxides, the fixed oxide charges were significantly reduced but the interface state density remained more or less the same. For low temperature (<600°C) H_2, N_2, and H_2O annealed oxides, both the interface state density and the fixed oxide density were significantly reduced. The reported lowest fixed oxide charge density is $-5.0x10^{10}/cm^2$ [4]. However, the reasons of observing those effects were not understood well. In this work, we attempt to explain the effects of segregated Ge on electrical properties of SiO_2/SiGe interface.

2. Experimental

Epitaxially grown undoped $Si_{1-x}Ge_x$ layers on an n-type (100) silicon substrate with Ge contents of 10%, 15%, and 20% were used for the experiment. The $Si_{1-x}Ge_x$ layers were oxidized in a furnace in H_2O ambient. For multi-step oxidation experiment, the previously grown surface oxide was removed in a diluted-HF solution. To observe annealing effects of thermal oxides, the samples were annealed at 1000°C in non-oxidizing N_2 ambient. To isolate the effects of segregated Ge on the interface electrical properties, an oxide grown by PECVD was also used. For PECVD oxides, the oxides were annealed in H_2 and N_2 ambient at 300°C for 30s. For C-V measurement, the backside of silicon substrate was thinned to 100μm to form a MOS capacitor and an aluminum gate electrode of an area 2.0×10^{-3} cm^2 was formed on top of the oxide layer.

3. Results and Discussions

The high frequency (1MHz) C-V curves for $Si_{0.85}Ge_{0.15}$ samples with multi-step oxidation and PECVD oxide are shown in Fig. 1. The thermal oxides show larger flat-band voltage shifts than the PECVD oxides, and the oxides after two thermal cycles show larger flat-band voltage shifts, while the PECVD oxides show little changes. From PECVD results, we can see that the segregated Ge itself does not influence to the fixed oxide charge density because the Ge content in the segregated region changes with the number of thermal cycles. The high temperature (1000°C for 120min. in N_2 ambient) annealing behaviors of a multi-step oxidized sample at 900°C for 10min. are shown in Fig. 2. After high temperature annealing, the flat-band voltages remain in the range of -0.36V to 0.13V for all the thermal cycled samples. Figure 3 shows a typical AES depth profiles for a wet oxidized $Si_{0.85}Ge_{0.15}$ sample. The Ge pileup at the interface is observed and the concentration of Ge in the oxide region is negligible. At the interface, we note that there is a dip in the Si profile. Before and after high temperature annealing, the XPS spectra for Si 2p and Ge 2p are measured for a 900°C thermally oxidized $Si_{0.9}Ge_{0.1}$ sample to observe the chemical bonding structures near the interface, and those are shown in Fig. 4. Two Si 2p peaks located at 99eV and 104eV originate from the bonding structures of SiGe alloy and SiO_2, respectively. The Ge 2p peak located at 1217eV originates from the elemental form of Ge. In the oxide region, the silicon exists in SiO_2 form and the Ge spectrum is negligible. At the interface, the elemental Ge peak increases without any core level shift as the amount of Ge pileup increases. The peak intensity for SiO_2 bonding is reduced and shows a core level shift toward the SiGe peak. Also, there exist shoulder peaks in the energy range of 100~104eV, indicating that significant amounts of suboxides exist. After annealing at 1000°C for 120min. in N_2 ambient, the length of the tail of SiO_2 peak is significantly reduced and the shoulder peaks for SiO_x are also reduced. The Si peak intensity versus sputter cycle for each bonding structure that is reduced from the XPS data is shown in Fig. 5. Here, we can clearly see an increase of SiGe bonds and the existence of SiO_x bonds, which are reduced after the high temperature annealing.

From these results and the known fact on oxidations of Si that the non-bridging oxygen bonds on a SiO_x structure take negative charge state, we can conclude that fixed negative charges exist in the Ge pileup region. This conclusion is also supported by the C-V characteristics in the depletion region of Fig. 1, where the capacitance of the 2 thermal cycle sample in the depletion region is higher than that of the 1 thermal cycle sample. The reduction of SiO_x after high temperature annealing results in the reduction of negative oxide charges observed in the high frequency C-V measurement.

References

[1] D.K. Nayak, J.S. Park, J.C.S. Woo, and K.L. Wang, J. Appl. Phys. 76(2) (1994) p 982.

[2] W.S. Liu, M.A. Nicolet, H.H. Park, B.H. Koak, and J.W. Lee, J. Appl. Phys. 78(4) (1995) p 2631.

[3] M. Mukhopadhyay, S.K. Ray, and C.K. Maiti, Appl. Phys. Lett. 65(7) (1994) p 895.

[4] D. Tchikatilov, Y.F. Yang, and E.S. Yang, Appl. Phys. Lett. 69(17) (1996) p 2578.

[5] A.A. Bright, J. Vac. Sci. Technol. A, 9(3) (1991) p 1088.

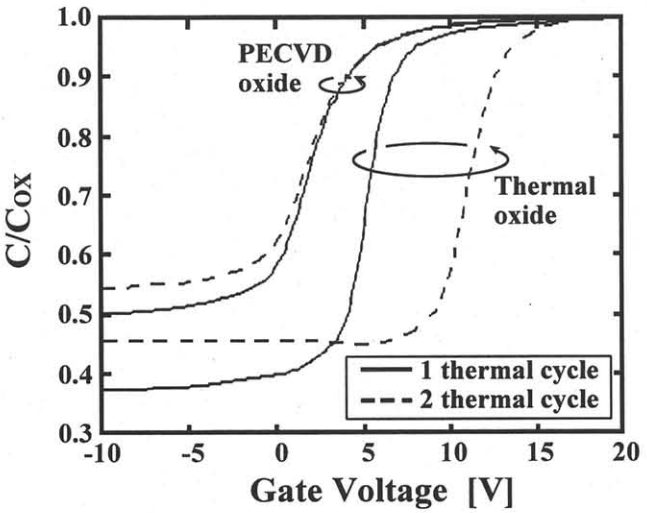

Fig. 1. High-frequency C-V curves for the multi-step oxidized $Si_{0.85}Ge_{0.15}$ alloys and for PECVD oxide-grown samples. After removal of previously grown oxides, a wet oxidation at 900°C for 10min or a PECVD SiO_2 deposition was followed.

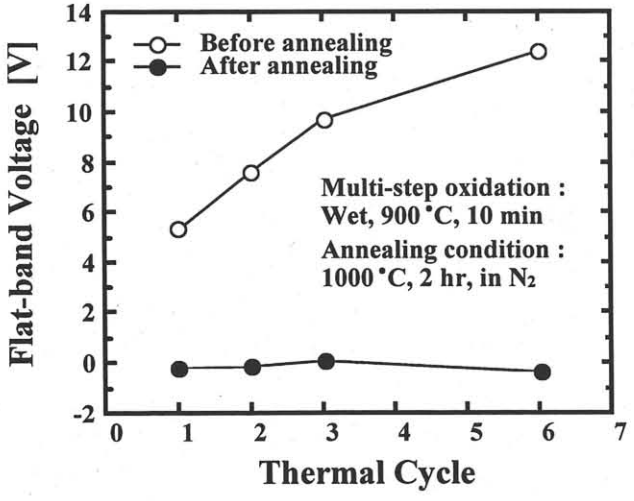

Fig. 2. The flat-band voltage versus thermal cycle of multi-step oxidized $Si_{0.9}Ge_{0.1}$ samples before and after annealing at 1000°C, in N_2 ambient for 120 min.

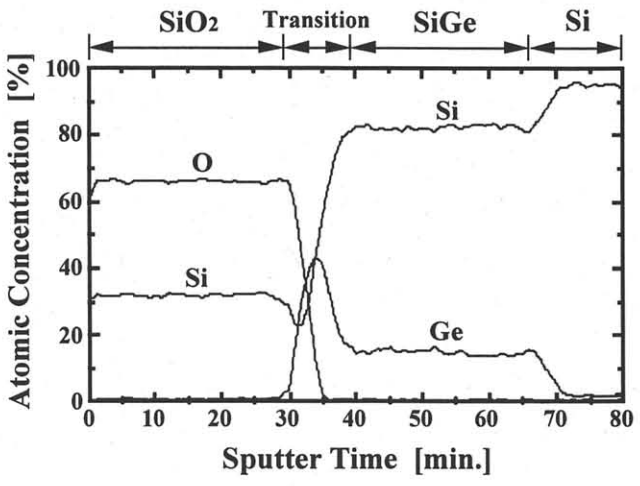

Fig. 3. The AES depth profile of a $Si_{0.85}Ge_{0.15}$ sample which is wet oxidized at 1000°C for 10 min.

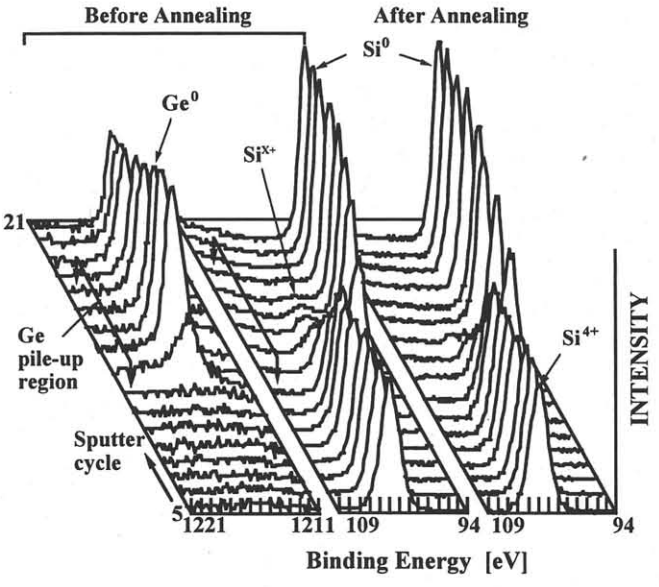

Fig. 4. XPS spectra of Si 2p and Ge 2p core level of the $Si_{0.9}Ge_{0.1}$ sample before and after annealing at 1000°C in N_2 for 120 min.

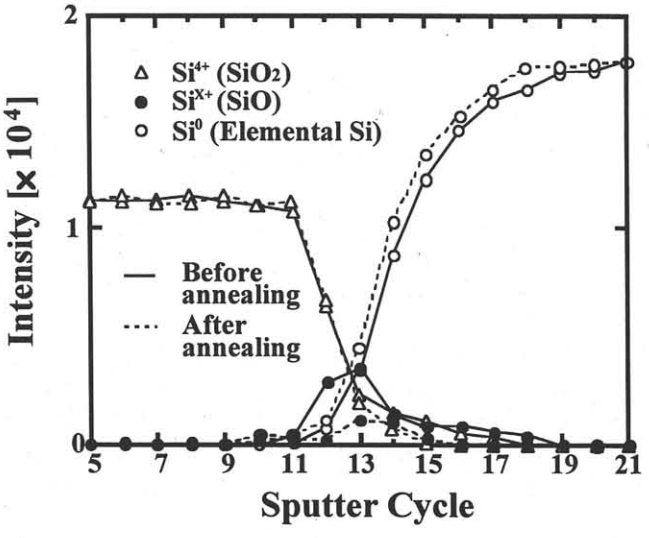

Fig. 5. XPS intensity profile of Si 2p core level for different bonding structures which are reduced from data in Fig. 4.