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Formation and Characterization of Thin Oxide Layers on the Spatially Controlled Atomic-Step-Free Si(001) Surface

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1. Introduction

The interface between SiO_2 and Si(001) is important for metal-oxide-semiconductor (MOS) devices.[1] As the gate oxide films become thinner, more precise control of the interface is necessary for reliability of the MOS character. It has been reported that oxidation of a clean Si(001) surface is affected by the surface roughness before the oxidation.[2] An atomic-step-free Si(001) surface is an ideal substrate, but it was difficult to obtain the surface whose area was large enough for device fabrication.

Recently, we have proposed a new technique for the spatially controlled formation of an atomic-step-free Si(001) surface at the desired position.[3, 4] The obtained surface has an area as large as several μm^2 and is an attractive platform for atomic-step-free MOS devices. In this paper, we demonstrate oxidation of the spatially controlled atomic-step-free Si(001) surface and characterize morphologies and local electrical properties of the SiO_2 / Si(001) structure by an atomic force microscope (AFM).

2. Experimental

A well-oriented Si(001) substrate (Shin-Etsu Semiconductors Co., Ltd.) was used for a specimen. Its surface normal was off from the [001] orientation by 0 - 7' along the [110] direction and by 3 - 7' along the [$\bar{1}$10] direction. For spatial control of atomic-step-free Si(001) surface, artificial step bands with depths of 20 - 500 nm were formed into square patterns by chemical etching.[3, 4] To obtain a large area of single atomic Si(001) terrace, the specimen was annealed at 1000°C by passing a direct current for 2 hours in an ultrahigh vacuum (UHV) system after the chemical and the thermal cleaning described previously.[3, 4] The pressure of the system was maintained in the order of 10^{-8} Pa during the annealing. The oxidation was successively performed in dry O_2 under a pressure of 2.0×10^{-4} Pa at 400 - 600°C for 10 min. The substrate temperature was monitored by a pyrometer.

Morphology of the oxidized surface was observed with an atmospheric AFM (SPA300, Seiko Instruments Inc.) just after unloading the specimen from the UHV system. Au coated cantilever with a microfabricated silicon nitride tip (Olympus Opt. Co., Ltd.) was used for the AFM observation. To evaluate the interface between SiO_2 and Si(001), the AFM observation was performed after the oxide layers were removed by dipping into a dilute HF solution and subsequently rinsed with ultrapure water. The root-mean-square (rms) values of roughness at the oxidized surface and the interface between SiO_2 and Si(001) were calculated from AFM topographies scanned over 640 x 640 nm^2 area on single atomic Si(001) terrace.

To characterize local electrical properties of the SiO_2 / Si(001) structure, two-dimensional current images and current-voltage curves were measured by the contact-mode AFM[5] with a Pt coated cantilever. The spatial resolution of this measurement is a few tens nm^2. The reference force during all AFM experiments was maintained in the order of 10^{-9} N.

3. Results and Discussion

The morphology of the oxidized surface was dependent on the oxidation condition. At the condition of high substrate temperature and low O_2 pressure, the surface etching occurred and there were a lot of pits with monoatomic-depth on the Si(001) terraces.[6] To avoid the etching which results in the surface roughening, it is necessary to start the oxidation at lower temperature than 400°C and to cool the oxidized specimen in an O_2 atmosphere.

The oxidized specimens free from the etching show similar morphology to that of the spatially controlled atomic-step-free Si(001) surface before the oxidation. The dependence of morphologies on the substrate temperature during the oxidation was not observed in the range of 400 -

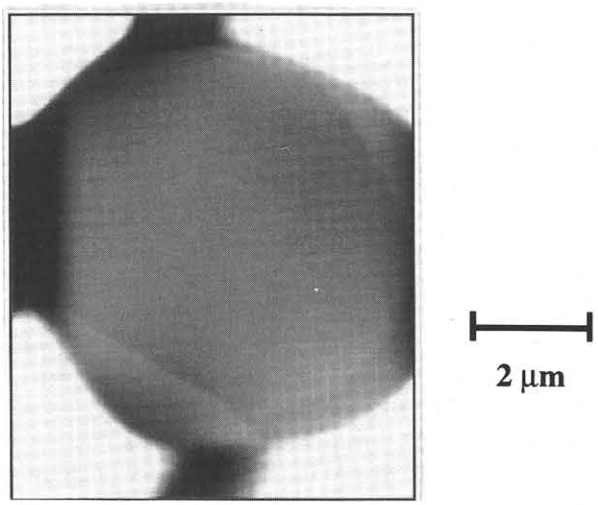

Fig. 1. 6.7 x 7.2 μm^2 AFM image of the Si(001) surface oxidized at 600°C.

600°C. Figure 1 shows a typical AFM image of the oxidized surface formed at 600°C. Single atomic Si(001) terrace of about 4 μm in diameter is observed. The rms roughness of the oxidized surface is about 0.055 nm and that of the interface between SiO_2 and Si(001) is 0.07 - 0.1 nm, which are small enough compared with a monoatomic step height (0.136 nm). These results suggest that an ideal SiO_2 / Si(001) structure can be obtained by the oxidation of the spatially controlled atomic-step-free Si(001) surface.

Although morphologies of the SiO_2 / Si(001) structures are independent of the substrate temperature during the oxidation in the range of 400 - 600°C, local electrical properties of the structure are affected by the temperatures. Figure 2 shows a two-dimensional current image obtained by scanning the cantilever at a sample bias voltage of -0.8 V. Contrast from white to black in Fig. 2 corresponds to the variation of current from small to large. Figure 3 shows current-voltage curves of the SiO_2 / Si(001) structure formed at 400°C, which were measured at seven different points. These figures indicate that there is a large spatial difference

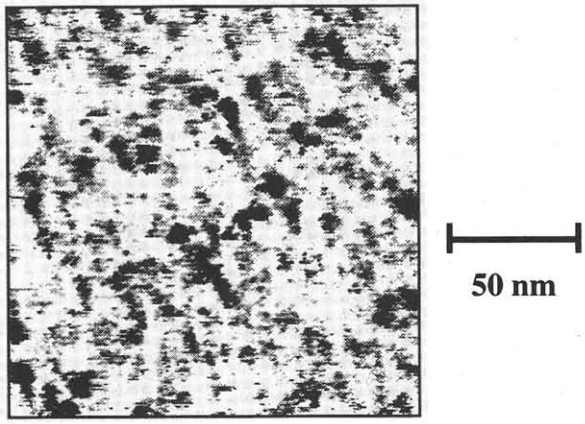

Fig. 2. 160 x 170 nm^2 two-dimensional current image of the SiO_2 / Si(001) structure formed at 400°C. The sample bias voltage was -0.8 V.

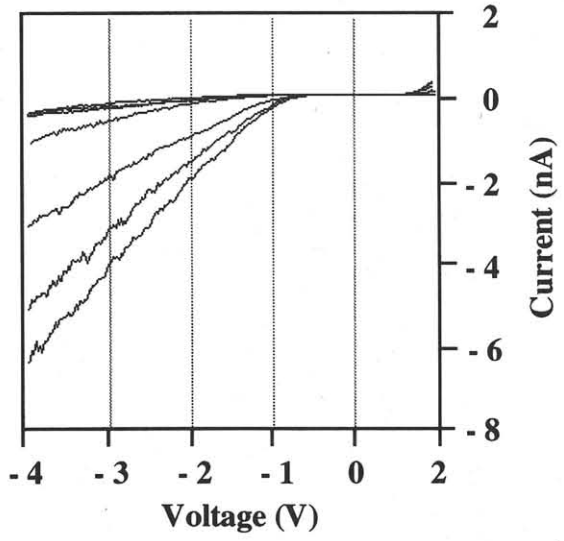

Fig. 3 Current-voltage curves of the SiO_2 / Si(001) structure formed at 400°C.

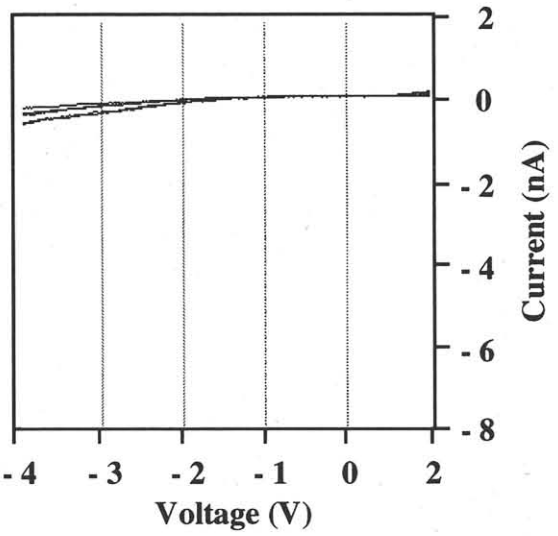

Fig. 4 Current-voltage curves of the SiO_2 / Si(001) structure formed at 600°C.

in the local electrical property of the SiO_2 / Si(001) structure formed at 400°C on a nanometer scale. As shown in Fig. 4, the uniformity in the local electrical property on a nanometer scale was improved when the SiO_2 / Si(001) structure was formed at 600°C. The variation of current at -4 V is reduced to 1/10 that of the SiO_2 / Si(001) structure formed at 400°C.

4. Conclusions

Oxidation of the spatially controlled atomic-step-free Si(001) surface and characterization of morphologies and local electrical properties of the SiO_2 / Si(001) structure have been demonstrated. An ideal SiO_2 / Si(001) structure with atomic-step-free surface and interface is obtained over an area of several μm^2. The oxidation temperature dependence of the uniformity of local electric properties was observed although morphologies were independent.

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