Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 392-393

Medium Field Breakdown Following Local Tunneling Current on MOS Capacitor Containing Grown-in CZ Crystal Defects

Masaro Tamatsuka, Zbigniew Radzimski*) and George A.Rozgonyi ,
Satoshi Oka [1], Masahiro Kato [1], and Yutaka Kitagawara [1]

Department of Materials Science and Engineering, North Carolina State University, Raleigh NC 27695-7916, USA
phone:+1-919-515-7217;fax:+1-919-515-5115;e-mail:tamatuka@mte.ncsu.edu
[1] SEH Isobe R&D Center, Shin-Etsu Handotai Co., Ltd. 2-13-1 Isobe, Annaka-Shi, Gunma-ken 379-01, Japan
*) Present address SEH America, Inc., 4111 Northeast 112th Avenue, Vancouver, WA 98682-6776, USA

1. Introduction

Gate dielectric strength is becoming more critical in advanced semiconductor devices; for example, flash memory functioning at high gate bias and highly integrated Metal Oxide Semiconductor (MOS) Random Access Memories (RAMs) requiring thinner gate oxide. For these devices, failure analysis of the origins of MOS breakdown is very important to clarify the relation between defects and MOS parameters such as gate materials, oxide thickness, and oxide quality [1]. Recently, grown-in crystal defects in Czochralski (CZ) silicon wafer have been widely reported. Crystal Originated Particles (COPs) [2], Flow Pattern Defects (FPDs) [3] and Laser Scattering Tomography Defects (LSTDs) [4] are typical grown-in defects detected in standard CZ silicon crystals grown at higher rate than ~1.0 mm/min. Although strong attention has been paid to these defects because of their correlation to Gate Oxide Integrity (GOI), the mechanism of oxide degradation is still not clear. This paper focuses on i) analyzing the local tunneling current flow mechanism at the defect site, ii) developing a procedure for characterizing the oxide defect after non-catastrophic breakdown, and iii) providing a model to clarify the origin and mechanism of medium field i.e. "B-mode" breakdown due to CZ crystal originated defects.

2. Experimental

The substrates used were six inch diameter [100] oriented boron doped CZ silicon wafers which are grown at regular rate of ~1.2 mm/min. Oxygen concentration was around 12 ppma (ASTM'80) and carbon concentration was below 0.05 ppma (ASTM'75). Thermal oxide was grown on the substrates in dry oxygen ambient at 900°C to 25nm thickness. Around 300 nm thickness Poly-Si gate film was deposited and patterned to fabricate over several hundred capacitor arrays. One hundred 20mm^2 area capacitors were examined on each wafer with an Hewlett Packard device tester. The breakdown voltage was defined as the applied negative gate bias voltage for which the leakage current abruptly goes up over 10mA. Following a statistical evaluation of the breakdown voltage distribution, some of 4 mm^2 area capacitors were selected as candidates for non-catastrophic breakdown test under 160 or 800 pA in order to insure with a minimum delineation induced damage. A High Resolution Scanning Electron Microscope / MOS / Electron Beam Induced Current (HRSEM/MOS/EBIC) imaging and a precise Carbon Whisker (CW) marking of the breakdown site in a JEOL JSM 6400F was followed by a Specific Area cross section Transmission Electron Microscopy (SAXTEM) sample preparation for a Topcon EM-002B using a Focused Ion Beam (FIB) (fei model 610) and dicing saw. Thus, a one-to-one identification of the morphology of the source of B-mode breakdown under sub-nano ampere current was possible.

3. Results and Discussion

The B-mode breakdown ratio of 20 mm^2 area capacitor was ~ 60 % corresponding oxide defects area density of 5 cm^{-2}. Local tunneling current was clearly observed in smaller 4 mm^2 area capacitors at the similar area density as shown in Fig. 1. The local effective oxide thinning (Δt_{ox}) and effective current emission area (A_{FN}) could be calculated assuming that the origin is local oxide thinning induced Fowler-Nordheim (F-N) tunneling current.

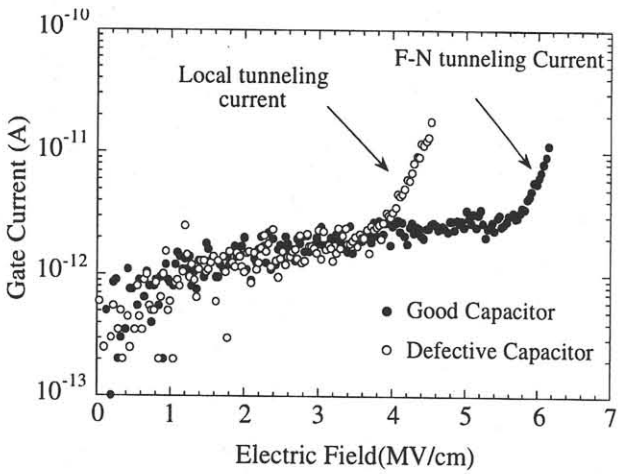

Fig. 1 Local tunneling on defective 4 mm2 area capacitor

Cross sectional TEM structural observation following a specific defect site localization and sample preparation technique is a powerful tool for analyzing low density oxide defects. So called copper decoration [5] and MOS/EBIC [6] method are commonly used for the delineation of grown-in oxide defects. In this study, high precision CW marking technique in HRSEM/MOS/EBIC was developed. A ~0.2μm size HRSEM/MOS/EBIC defect image on a 4 mm^2 area capacitor which was broken down at 160 pA stress current was clearly seen without any surface feature on the gate film surface at the same position in SEM mode, see Fig. 2.

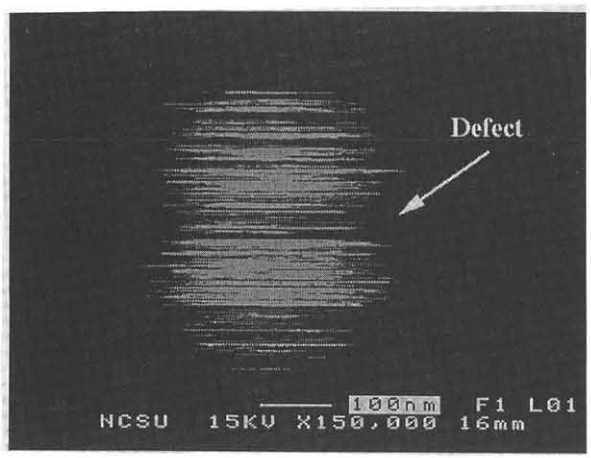

Fig. 2 HRSEM/EBIC leakage site image

A CW mark was grown within a few minute by focusing an electron beam on the EBIC image site at high magnification. This CW mark was easily visible in FIB milling machine with the navigation scratch mark putted by EBIC probe, see Fig. 3. This procedure provide ± 0.1 μm precision of detecting the oxide defects in a SAXTEM sample.

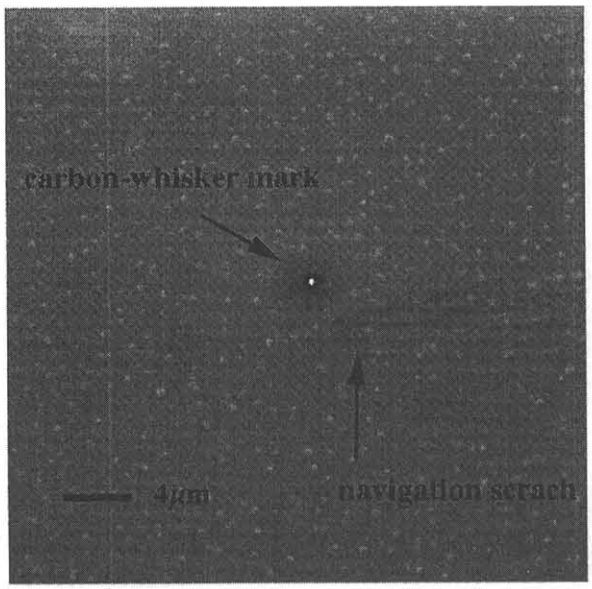

Fig. 3 CW mark observed in FIB

There are many mechanism for explaining breakdown mechanism due to grown-in oxide defects. They are a) local oxide thinning, b) barrier height lowering c) charge trap in the oxide due to contamination, and d) morphological emission efficiency increase (shape effect). From a direct TEM observation of a grown-in oxide defect which broken down by 800 pA stress, where the breakdown induced damage is much more limited than in typical breakdown test, see Fig. 4. Although the defect was partially damaged by charge dispersion energy, especially at the top and bottom side corners, an octahedral defect was clearly seen as the origin of oxide breakdown. Further TEM analysis including lower 160 pA stress current samples could clarify the oxide breakdown mechanism due to grown-in oxide defects.

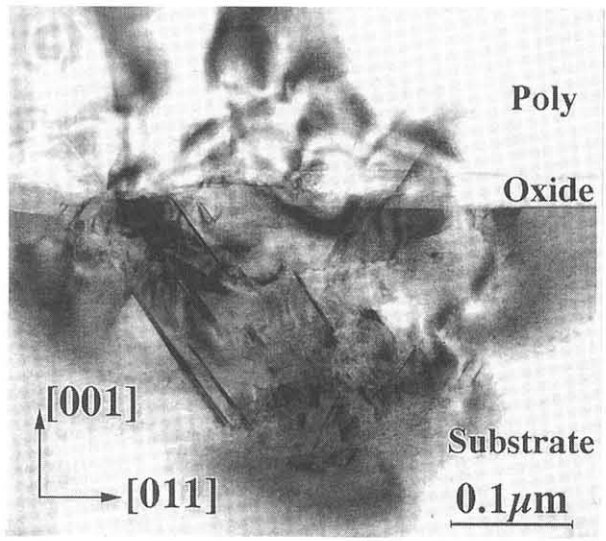

Fig. 4 X-TEM image of broken down grown-in oxide defect

4. Conclusions

It has been shown that local tunneling current followed by B-mode breakdown was clearly observed in a 4 mm^2 area capacitor at a typical area density for as-grown CZ wafers. The breakdown site, even using currents as low as 160 pA, is clearly visible at ~0.2 μm size in the HRSEM/MOS/EBIC imaging mode. These sites were precisely marked by growing a carbon-whisker in HRSEM and SAXTEM sample preparation was done by FIB and dicing saw. It was found that the origin of B-mode breakdown on as-grown CZ wafers is the same octahedral type defect which was observed by Itsumi, et al (5).

Acknowledgments

This work was supported by Shin-Etsu Handotai Co. Ltd.,(SEH).

References

1. R.Sugino, T.Nakanishi, K.Takasaki, and T.Ito, J.Electrochem. Soc., 143, 2691 (1996).
2. J.Ryuta, E.Morita, T.Tanaka, and Y.Shimanuki, Jpn.J.Appl.Phys. 29, L1947 (1990)
3. H.Yamagishi, I.Fusegawa, N.Fujimaki, and M.Katayama, Semicond. Sci. Technol. 7, A135 (1992)
4. Y.Kitagawara, K.Aihara, S.Oka, and T.Takenaka, Materials Science Forum Vols. 196-201, 1835 (1995) Trans Tech Publications, Switzerland
5. M.Itsumi, H.Akiya, and T.Ueki, J.Appl.Phys.78, 5984 (1995)
6. J-G.Park, H.Kirk, C-S.Lee, H-K.Lee, D-M.Lee and G.A.Rozgonyi, Semiconductor Silicon/1994, ed H.R.Huff, W.Bergholz and K.Sumino, PV94-10, 370 (1994) The ECSProc. Series, Pennington,NJ