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Influence of Wafer Material on Defect Generation During Deep Submicron LOCOS Process

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1. Introduction

Suppression of bird's beak encroachment is a critical issue for the deep submicron LOCOS. The encroachment can be suppressed by the combination of thick silicon nitride(Si_3N_4) and thin pad oxide. For example, 0.2 μm isolation was realized by the conventional LOCOS process[1]. However, the bird's beak suppression tends to increase in stress and generate a variety of defects in Si[2,3]. Since the generation of oxidation-induced defects is associated with Si wafer characteristics[4], not only LOCOS parameters but also the Si wafer specifics should be paid attention.

In this paper, observation of defects induced by the deep submicron LOCOS process is described. The relationships between Si wafer characteristics and defect types and densities are discussed.

2. Experimental

Four types of widely used wafer materials were chosen: a standard Czochralski(CZ) wafer, a CZ wafer with denuded zone-intrinsic gettering(DZIG) treatment, a CZ wafer with polysilicon back sealing layer(PBS) and a CZ wafer grown in a magnetic field(MCZ). The specifications of these wafers are summarized in Table I.

Experimental procedures are explained in Fig. 1. Thermal oxide was grown to 5 nm thick as the pad oxide at 1000 °C in dry O_2, followed by 220 nm Si_3N_4 deposition at 750 °C by an LPCVD method. After the patterning of Si_3N_4 by a reactive ion etching method, field oxide was grown to a thickness of 300 nm at 1100 °C by a pyrogenic technique.

The oxidation induced defects were observed as etch pits after Wright etching of specimens. The field oxide and Si_3N_4 were usually removed prior to the Wright etching to observe the defects locating under the field oxide(Fig. 1(c)).

3. Results and Discussions

Figure 2 shows the cross-section of a 250 nm-width field oxide fabricated with the CZ wafer. Bird's beaks are sufficiently small for deep submicron isolation. However, the many etch pits which are attributed to oxidation induced defects are observed as prospected. For the quantitative defect evaluation, etch pits within line and space patterns (L/S) formed with field oxides were observed. Plan view micrographs and summary of the etch pit densities are shown in Figs. 3 and 4, respectively.

In the cases of the CZ and the PBS wafers, many etch pits are observed, whereas the etch pits are hardly observed in the cases of the DZIG and the MCZ wafers. The etch pit densities decrease down to 50 % for the PBS wafer and less than 1 % for the DZIG and the MCZ wafers as compared with the CZ wafer. In addition, it is clear that as the L/S pitch becomes larger, the etch pit densities increase. Our previous experiments indicate that the stress on Si substrates gets stronger as the Si_3N_4 width and the field oxide thickness increase[5]. Oxygen concentrations in the CZ and the PBS wafers exceed 1.35×10^{18} cm^{-3} as Table I, which means that supersaturated oxygen in these wafers easily precipitates as SiO_2 during high temperature processes like oxidation. Such precipitation often works as the origin of defect formation accompanied with strong stress due to the LOCOS process. The observed etch pits are considered to correspond to dislocations generated in this way. Different from the CZ and the PBS wafers, DZIG wafers have low oxygen concentration region at the wafer surface and the MCZ wafer contains less oxygen than the others as Table I. In addition, MCZ wafers generally contain excess interstitial Si, which also suppress the SiO_2 precipitation[6]. Thus, it seems that the SiO_2 precipitation around the Si surface is the key to the etch pit density reduction.

The plan-view micrographs for an isolated field oxide line are shown in Fig. 5. Width of Si_3N_4 on both sides of the isolated field oxide is 20 μm. In contrast to the L/S cases, stacking faults are observed for the DZIG and the MCZ wafers. The etch pits, namely dislocations, are observed for the CZ and the PBS wafers as well as the L/S. The stress around the isolated field oxide with wide Si_3N_4 is higher than that around L/S patterns[7]. The stress in wafers is generally released by defect formation. In the case of the CZ and the PBS wafers, the stress was released by the generations of many dislocations. However, in the DZIG and the MCZ wafers, since the dislocation formation is suppressed as explained above, the stress triggers off stacking faults formation. LOCOS parameter modification, e.g. reduction in oxidation time and thickness, will weaken the stress and reduce the stacking faults.

4. Conclusions

Influence of Si wafers on defects generation during LOCOS process for the deep submicron isolation has been investigated using the various Si wafers. The defects densities were successfully reduced by using the DZIG and the MCZ wafers, probably because of suppression of the SiO_2 precipitation. In the isolated field oxide patterns,

however, the stress in Si substrates was so strong that the stacking faults were introduced even in the DZIG and the MCZ wafers.

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Table I Specifications of the used Si wafers.

Si wafers	As-grown oxygen concentration	Other specifications
CZ	1.35-1.55×10^{18} cm^{-3}	*p*-type (B doped) 8.5-11.5 Ω·cm (100)-oriented
DZIG		
PBS		
MCZ	less than 1.0×10^{18} cm^{-3}	

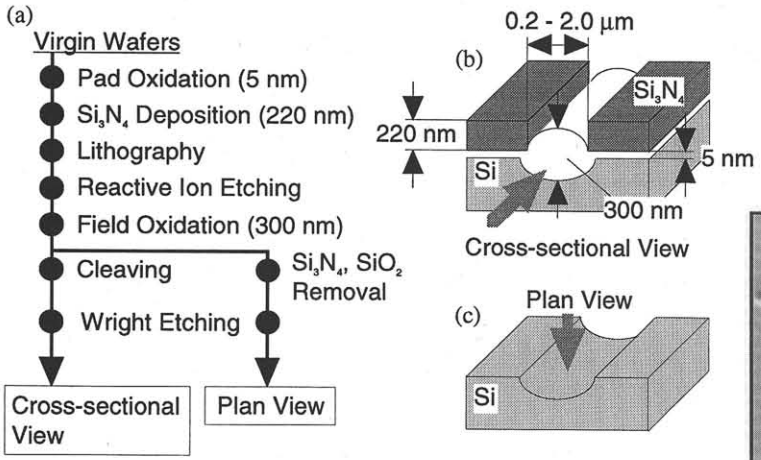

Fig. 1 (a) Experimental procedures. Schematics of specimens for (b) cross-section view and (c) plan view.

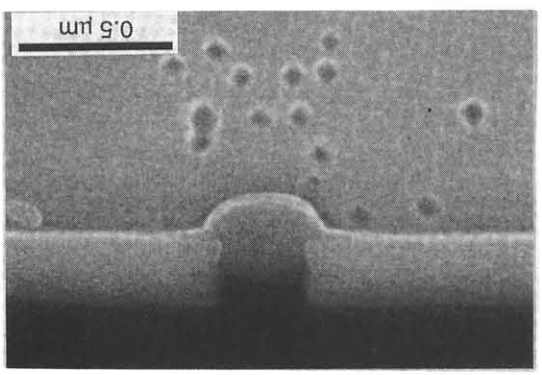

Fig. 2 SEM micrograph of a 250 nm-width field oxide pattern.

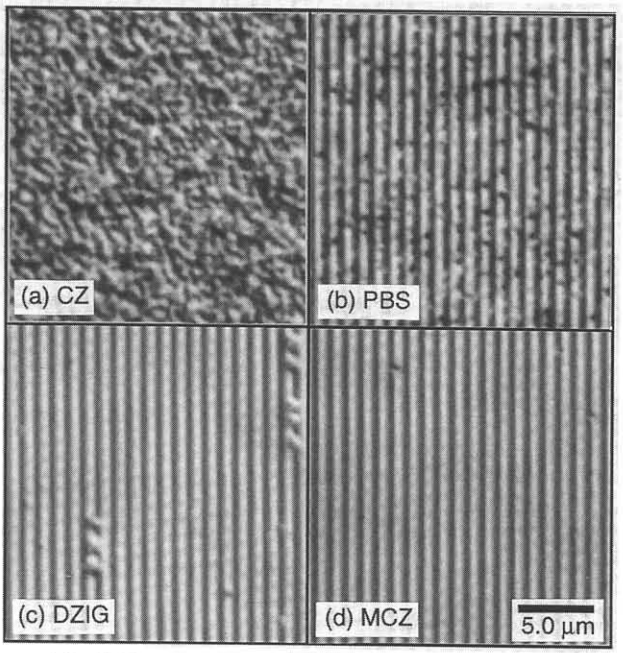

Fig. 3 Plan views around 0.5 μm-width L/S patterns.

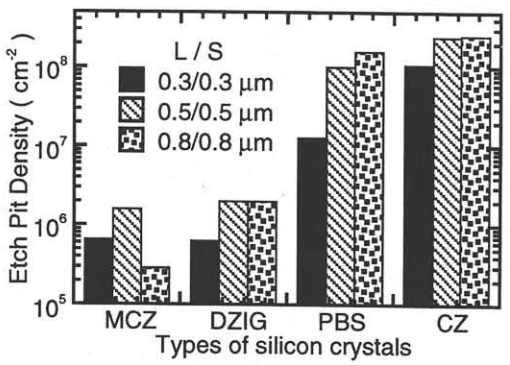

Fig. 4 The etch pit densities obtained with the same specimens as those for Fig. 3.

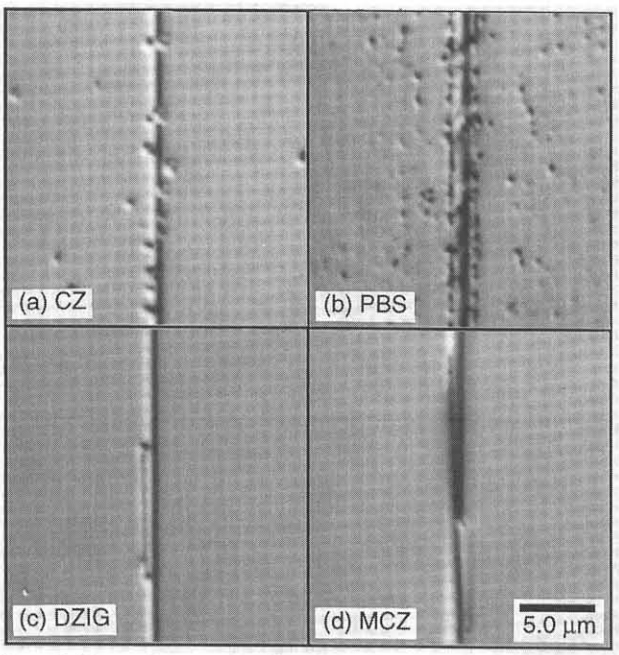

Fig. 5 Plan views around a 0.5 μm-width isolated line. Stacking faults are observed as "etch lines" for the DZIG and MCZ wafers.