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The Analysis of Defective Cell Induced by COP in 0.3 microns Technology Node DRAM

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1. Introduction

From the investigation of DRAM memory cells in 0.3 microns process TEG (Test Element Group), the influence of COP(Crystal Originated Pit) on the memory cell was clarified. COP constrains the field oxide to grow and brings degradation on isolation characteristics between adjacent memory cells.

Recently many papers have been reporting the study of COP on the surface of CZ wafer especially in the deep sub-micron devices[1)2)]. As far as the deep sub-micron DRAM is concerned, the design rule which the latest manufacturing DRAM employs is comparable to COP in dimension. Consequently COP will be a big issue in the yield and reliability degradation. The concrete problem of COP is the degradation of some electrical features, such as isolation characteristics between the adjacent cells , junction leakage and the MOS transistor principally.

In this study, we tested the memory cells in the TEG which can operate as actual DRAM. The following is our list of findings, including the density of COP, the electrical characteristics of the defective memory cell, the physical analysis and finally the conceivable failure mechanism.

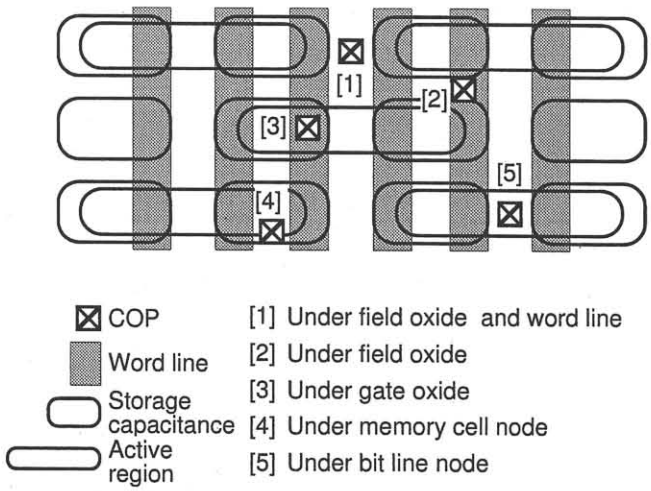

Fig. 1 Location of COP in DRAM memory cell.

2. Experimental

Modeling

Fig. 1 shows the placements of COP in DRAM memory array where COP may ruin the memory cells. The following failure models are likely to take place.

In case of [1] and [2], COP is located under the field oxide, it induces the degradation of isolation characteristics between memory cells, one of the most important factors of DRAM. However, the case of [2] is more serious than [1] because of overlapping with the adjacent word line.

In case of [3], COP is located under the gate oxide , the feature of transfer MOS transistor degrades due to thinness of the gate oxide.

In case of [4], COP is located close to or touches the depletion region of p-n junction, the junction leakage current increases due to enhancement of the interface traps and electric field.

In case of [5], COP is located under bit line node, memory cells which share common contact hall fail due to the disconnection.

Testing Method

The memory cells were tested by the same testing technique as actual DRAM, to read the cell data after 100-ms pause, by using sense amplifiers equipped in the TEG, and were sorted into three defect modes under the conditions shown in Table I. We tested two materials, CZ and Epitaxy of 1 micron vapor-phase growth wafer.

3. Results and Discussion

Results

All defective cells , sorted by the mentioned technique , were observed with SEM. As a result, the print of COP retaining pyramidal (half of octahedral) shape was only observed under isolations test condition and in CZ wafer , as shown in Table I. Every print was located under the field oxide and word line as SEM micrograph shown in Fig. 2. This print plunges into the defective cell , whereas this cell didn't fail under junction test conditions. It suggests that COP doesn't always happen to increase junction leakage strikingly.

Another memory cell adjacent to COP as [1] in Fig. 1, which had been found out with Defect Inspection System just after field oxide forming, wasn't detected under any test conditions.

Analysis

The surface density of COP on the CZ wafer can be estimated by determining how many failures exist in the area where the field oxide and word line are overlapping. The density is 1 - 2/cm^2.

Fig. 3 shows the features of the leakage current versus Vsub(Substrate voltage) and Vgate(Word line voltage) of the defective cell similar to Fig. 2 in shape. This current is calculated with the reciprocal number of Retention Time. Retention Time is a minimum time length in which the memory cell can retain the data.

Table I Experimental result of defect density of COP and test conditions.

Material	Isolation leakage (pit /cm^2)	Junction leakage (pit /cm^2)	MOS degradation (pit /cm^2)
CZ	1 ~ 2	0	0
Epitaxy	0	0	0
Conditions			
Vword(adjacent)	5.0V	0.0V	0.0V
Vsub	-0.4V	-3.0V	-0.4V
Retention Time	100ms	100ms	100ms

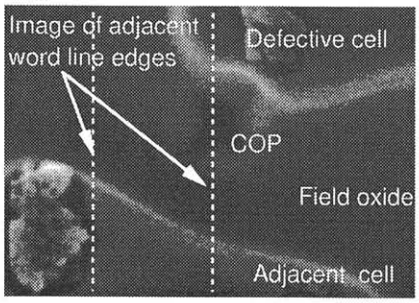

Fig. 2 Plane-view SEM micrograph of the print of COP between adjacent cells and under the field oxide and adjacent word line, after removing the field oxide.

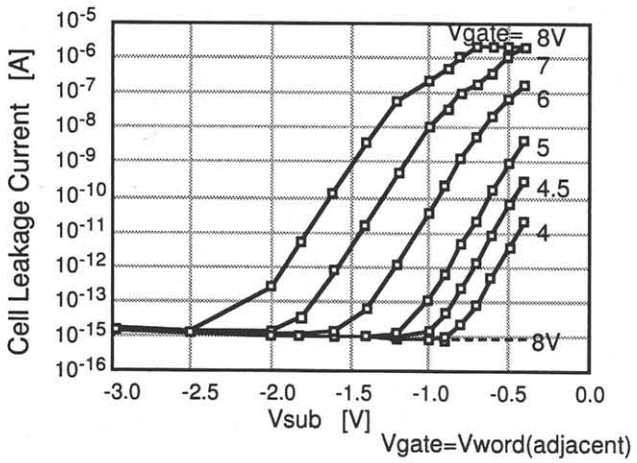

Fig. 3 Leakage current dependency on Vsub/Vgate of defective cell by COP (solid line) and non-defective cell's (dotted line).

Discussion

In Fig. 3, the leakage current of a non-defective cell shows reverse leakage current characteristics of p-n junction.

However, the leakage current of defective cell increases exponentially when Vsub varies to a shallower side and/or Vgate varies to a higher side, and differs from the non-defective cell's remarkably. It is a conceived subthreshold current behavior[3] of field oxide.

Fig.4 shows the cross-sectional SEM micrograph of the field oxide in another place. The field oxide is sunk, and this depression is so similar to the print in Fig .2 in size and shape, that it must be caused by COP. And further, the field oxide is thinner around this depression and the thinnest at the center by less than half of which is typical.

Eventually, the mechanism of how COP induces the degradation of isolation characteristics between the memory cells can be explained with two factors as follows.

(1)The field oxide is constrained to grow due to COP and formed thinner in fabrication. The possible reason of the constraint is the nitride filling in COP acts as the mask of field oxide forming.

(2)Due to this structure, the channel stopper is implanted so deep through the field oxide, that the concentration N_A just under the field oxide becomes lower.

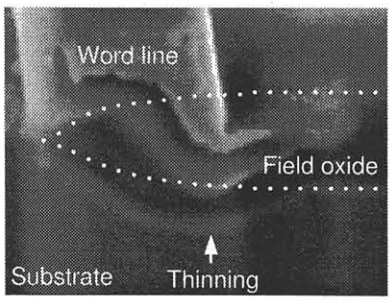

Fig. 4 Cross-sectional SEM micrograph of the print of COP at the field oxide and typical shape(dotted line).

The field oxide thinning and low concentration causes an increase in the subthreshold current.

Finally, in DRAM operation, when the word line adjacent to the defective cell activates, the subthreshold current increases drastically and the storage charge in the memory cell leaks to the adjacent cell.

4. Conclusion

From our investigation of DRAM memory cell in 0.3 microns process TEG, COP was found only in the CZ wafer but never in the Epitaxy wafer, and only induced the degradation of isolation characteristics because of a drastic increase of subthreshold leakage between the adjacent memory cells. The reason of the increase is COP constrains the field oxide to grow around itself in fabrication.

References

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