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High-Speed and Low-Power D-FF Employing MOBILEs (Monostable-Bistable Transition Logic Elements)

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1. Introduction

Resonant tunneling devices have been considered a possible candidate for the key device in the near future and have therefore been intensively studied in recent years. This is due to the potential for high-speed operation of resonant tunneling devices as well as their high functionality, which leads to lower power dissipation. We have developed a new logic gate, called a MOBILE (monostable-bistable transition logic element), which exploits the negative differential resistance (NDR) of the resonant tunneling phenomenon [1]. High-speed operations up to 18 Gb/s of the MOBILE inverter have been recently demonstrated at room temperature [2]. This paper proposes a novel delayed flip-flop (D-FF) circuit using MOBILEs, which has the compatible function with that of the ordinary D-FF and demonstrates a high-speed and low-power operation up to 12.5 Gb/s at room temperature.

2. Monostable-bistable transition logic elements

The operating principle of a MOBILE is explained in Fig. 1. It has two aspects: 1) employing the monostable-to-bistable transition of a circuit consisting of two NDR devices connected serially, and 2) driving this circuit by oscillating the bias voltage (V_{bias}) to produce the transition. A stable point in the $V_{bias}<2V_p$ region splits into two branches when V_{bias} increases through $2V_p$. A small difference in the peak currents of the two NDR devices determines the circuit's state after the transition. The circuit therefore forms a logic gate with the oscillatory varying of the bias voltage, which acts as a clock.

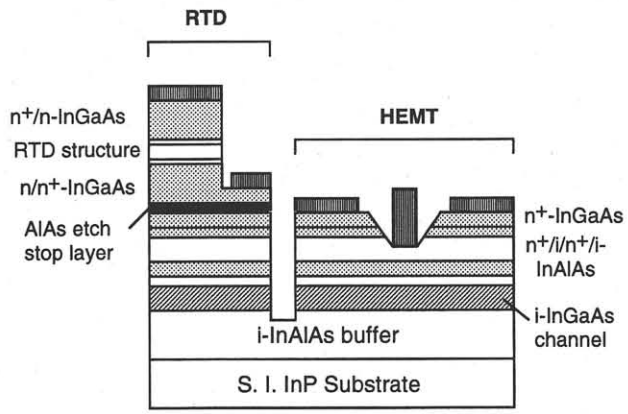

Fig. 2. Schematic cross section of the fabricated devices.

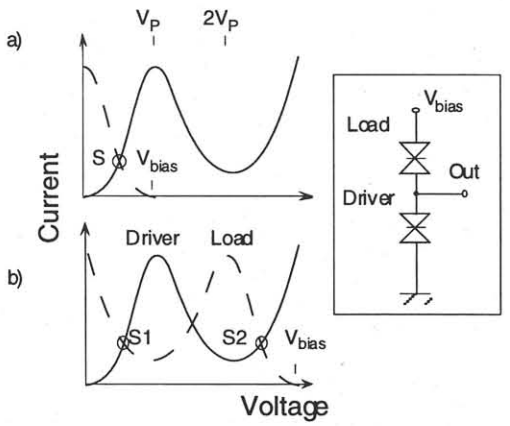

Fig. 1. The operating principle of the MOBILE. The figures on the left are load line diagrams and the one on the right shows the connection of the NDR devices. In the left-hand figure the solid line shows the *I-V* curve of the driver device and the dashed line shows the load line. (a) $V_{bias} < 2V_p$ (b) $V_{bias} > 2V_p$.

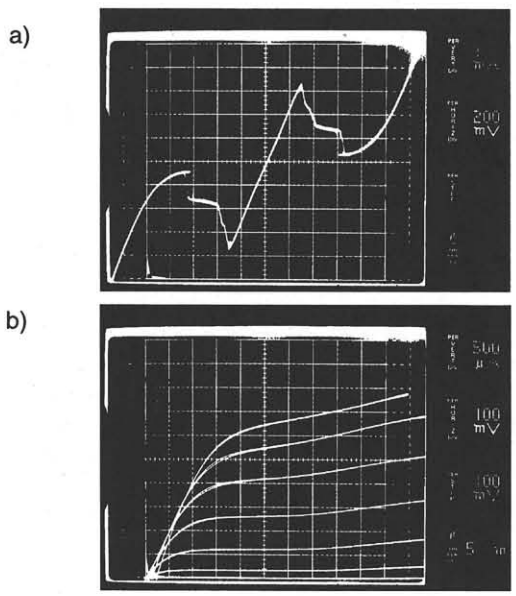

Fig. 3. The *I-V* characteristics of a) RTD and b) HEMT at room temperature. The size of the RTD is 2x2 µm². The maximum gate voltage is 0.7 V with a 0.1 V step. The gate length and width are 0.7 and 10 µm.

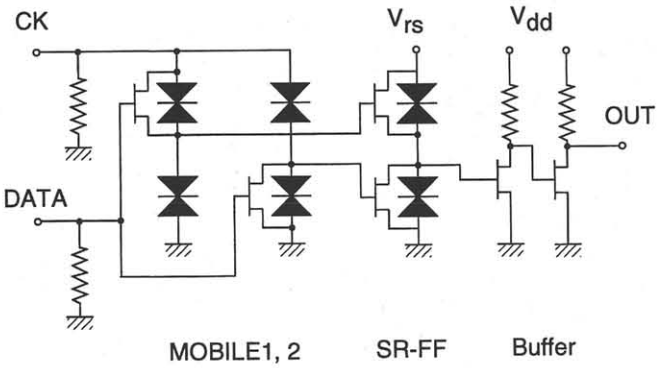

Fig. 4. Circuit configuration of the proposed D-FF. The MOBILE2 has an extra HEMT parallel to the lower RTD for controling the threshold (not shown).

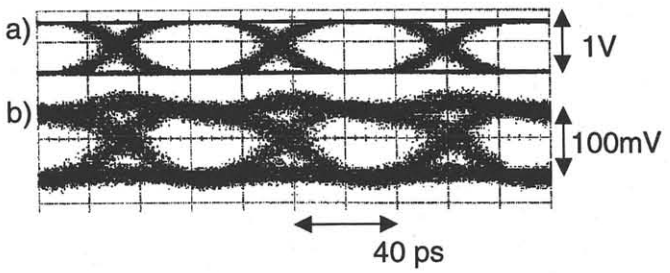

Fig. 5. The input (a) and output (b) eye patterns at 12.5 Gb/s.

A parallel circuit of a resonant tunneling diode (RTD) and a HEMT was used as a basic NDR device capable of peak-current modulation; it was fabricated using the InP-based RTD/HEMT integration technology [3]. The schematic cross section of the fabricated devices is shown in Fig. 2. The *I-V* characteristics of the fabricated RTD and the HEMT are shown in Fig. 3. The current density of the RTD was 8×10^4 A/cm^2. The gate length and the cutoff frequency f_T of the HEMT used were 0.7 μm and 40 GHz.

3. Circuit configuration

Figure 4 shows the circuit configuration of the fabricated D-FF. This D-FF consists of two MOBILEs and a set/reset flip-flop (SR-FF). This SR-FF also consists of a serially-connected RTD pair with HEMTs but is driven by a dc voltage [4]. The areas of the RTDs in the SR-FF are designed to be relatively small so that the HEMTs can switch the circuit's state between two stable states without oscillation of the bias voltage. This RTD pair circuit works therefore as an SR-FF, though the circuit configuration is similar to that of MOBILEs. It should be noted, on the other hand, that MOBILEs switch states only at the rising edge of the clock (bias voltage) and maintain their states while the clock is high. The operation of the proposed D-FF circuit is explained as follows. In the first stage, according to the input data just when the clock rises, a MOBILE with an input attached to the lower RTD generates a reset pulse, or another MOBILE with an input attached to the upper RTD generates a set pulse. Those pulses then switch the SR-FF, and the data are stored in it. Consequently, the circuit works as a D-FF. The number of devices for the core circuit (two MOBILEs and an SR-FF) of the D-FF is reduced to only ten, which is one-third of that of conventional SCFL D-FFs.

4. Circuit operation

A 2^{31}-1 PRBS (pseudo-random bit stream) from a pulse pattern generator was fed to the fabricated circuit. Then the output signal was amplified and tested by an error detector. Error-free operation (bit error rate less than 10^{-9}) was confirmed at bit rates up to 12.5 Gb/s. Figure 5 shows the output eye-pattern at 12.5 Gb/s. An even higher operation bit rate, close to the f_T of the HEMT used, is expected after the optimization of the circuit design, since there is no feedback loop and the intrinsic switching speed of the RTD is much higher [5].

This circuit uses a clock pulse as an oscillating bias voltage for MOBILEs so that measuring the power consumption is not straightforward. The power consumption estimated from individual devices is as small as about 10 mW for the core circuit of the D-FF. This value is less than one-tenth of those of the conventional D-FFs. It should be noted that the capacitance of the RTDs is so small that the dynamic current is small compared to the static current at frequencies up to a few tenths of gigahertz. This indicates the power consumption in the RTDs remains nearly constant in this frequency range. This fact and the reduction of the circuit complexity suggests that the RTD circuits are promising for high-speed and low-power digital ICs.

5. Conclusion

A novel D-FF using MOBILEs was proposed and fabricated with the InP-based RTD/HEMT integration technology. A high-speed operation at 12.5 Gb/s was demonstrated using HEMTs with a relatively large gate length of 0.7 μm. This result in conjunction with the low power consumption indicates the promise of the MOBILE-based high-speed digital circuits.

Acknowledgments

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References

1) K. Maezawa, T. Akeyoshi and T. Mizutani: IEEE Tran. Electron Devices, **41** (1994) 148.
2) K. Maezawa, H. Matsuzaki, K. Arai, T. Otsuji and M. Yamamoto: *to be presented at DRC '97.*
3) K. J. Chen, K. Maezawa and M. Yamamoto: IEEE Electron Device Lett. **17** (1996) 127.
4) K. J. Chen, T. Akeyoshi and K. Maezawa: Electronics Lett. **30** (1994) 1805.
5) N. Shimizu, T. Nagatsuma, T. Waho, M. Shinagawa, M. Yaita and M. Yamamoto: Electronics Lett. **31** (1995) 1695.