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Invited

Silicon-Based IC Technology for Giga-Scale Integration Era

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1. Introduction

As a main stream technology for integrated circuits, silicon technology has made remarkable progress in the past four decades since Kilby's invention: $10^{6\sim8}$x in active device counts per chip, $10^{6\sim8}$x in switching speed and $10^{5\sim7}$x in cost per function or bit.

Such progress has been largely supported by evolution of lithography capability, invention of MOS transistors with self-aligned gate followed by CMOS ICs, better understanding of materials, processing, and device physics leading to continuous improvement in manufacturing technologies. Circuit innovations such as dynamic logic and memory circuitries should also be credited to for the significant progress.

When we look at the future of silicon-based IC technology, a fundamental question to be asked would be how far can we proceed at the same pace as in the past. In other words, can we move with all of technology fronts, balanced and consistent to each other, in order to keep "Moore's Law" as the guiding principle? Another key question would be, how can we best utilize those enabling technology capabilities for implementation in new products on the horizon which would bring enough value back to sustain ever increasing silicon technology R&D investment levels.

The purpose of this paper is to focus on technical aspects of those questions from the viewpoint of device, process and materials viewpoints.

2. Technology Driving Products

Computing systems always have been behind the progress of IC technology. Fig. 1 illustrates a rather simplified view of how migration of computing power has taken place from mainframe systems to handheld systems, supported by a variety of enabling technologies. Capability of computing, once in the mainframe system, is now almost in the handheld system. Ultimately more than computing capability will be in the handheld category with multimedia/communication applications emerging. Among technologies which have allowed these changes, IC technology, in terms of hardware implementation of systems and even software as embedded in silicon chip, is the key enabler. IC technology always has made a more sophisticated system or subsystem on a smaller silicon chip at a lower cost. In other words, evolution of silicon technology has constantly contributed to industrial productivity improvement. As discussed elsewhere[1] the broad spectrum of IC technology, consisting of design, process, material, tools for manufacturing, needs a technology driver by which all technology fronts can be orchestrated in their pace of progress. It has been well accepted that Dynamic Random Access Memory (DRAM) was the technology driver until the early 1990s, followed by microprocessors which started playing a dominant role in development of multilevel on-chip interconnection technology. From the middle of the 1990s, exploding applications in the areas of wireless, handheld systems have strongly driven "low power consumption" CMOS technology for battery powered systems which may prompt utilization of SOI structures. The common characteristics of these technology drivers are the requirement for higher density on chip, higher performance and lower cost per bit or function. All of which are the reasons for the existence of integrated circuits.

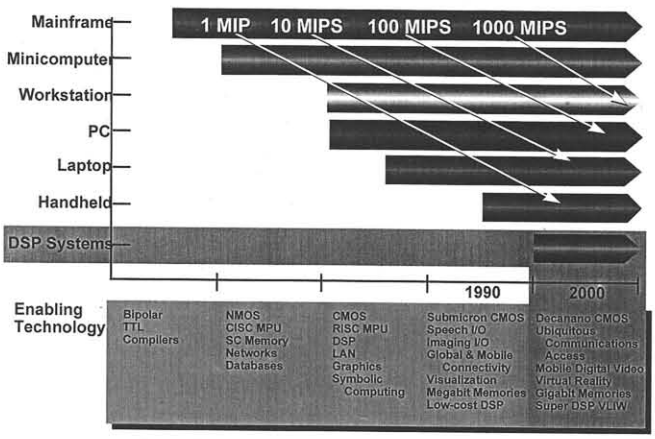

Fig. 1 Moving Power to the Person

3. Device and Process Technology

MOS Transistor

A large number of studies[2345][6] have been published for sub-0.1μm MOSFETs, covering basic device performances such as V_G-I_D characteristics, the short channel effect for the threshold voltage, the subthreshold behavior of current characteristics, and more fabrication oriented issues such as formation of gate insulator and its integrity, shallow source and drain region with improved resistivity. Deeper understanding of device physics has led to more precise prediction of MOSFETs with sub-0.1μm channel length and reliability design capability. However, such questions as whether we can practically

utilize gate oxide thickness of 1.5nm - 2.0nm where the through-oxide tunneling current becomes non-negligible and the gate oxide integrity sensitive to tunneling mechanism is unanswered; i.e., Fowler-Nordheim versus direct tunneling. Another frequently raised question is, how can we possibly replace the gate insulator with some type of new material that has higher dielectric constant, is SiO_2 equivalent, and controlled interface with silicon, desirably, free from 400°C hydrogen annealing.

On-Chip Interconnect

For Giga-scale integration, RC delay, signal crosstalk, power consumed through charge-discharge cycle and electromigration will be the most significant bottleneck. This bottleneck could be much more serious than any active device issues. Current trends toward adoption of new insulators with lower dielectric constant and copper-based metal certainly provide some relief for this problem. At the same time, "clever" interconnect design, consisting of proper selection for the number of interconnect layers and insertion of repeaters under the constraint of process and design cost will become increasingly important[78]. It is suspicious whether those efforts are good enough to deal with highly dense interconnections. Some futuristic thought would be to introduce on-chip optical interconnect, though immediate difficulty in light transmitter would place serious restriction to broader application of the technology even under optimistic assumptions for optical waveguide and detector. Pragmatic compromise will be the hybridization of electrical and optical interconnect.

Microfabrication Technologies

Optical lithography, in broader definition, has been a basic platform of IC manufacturing allowing us to shrink the minimum geometry by 0.7x in every technology generation, down to 0.18μm.

There is some belief that ArF laser-based lithography will enable 0.13 - 0.12μm with resolution enhancement as shown in Fig. 2. Extreme UV, X-ray, ion beam and electron beam, which utilize masked parallel write or direct serial write electron beam and ion beam technologies, have been pursued in order to establish "post-optical" position for sub-0.1μm geometry domain. It is again unclear which of those candidates will become the cost effective solution. As compared to X-ray and direct write electron beam, EUV and Scalpel technologies are receiving more attention today due to their rapid progress. A common concern, however, still resides in the area of mask technology, which is ironically the same bottleneck as X-ray technology has suffered for many years.

Film deposition and etch technology coupled with either selective doping of impurities into silicon or topography formation for transistors and interconnects have made excellent progress in recent years. Better understanding of plasma chemistry, and therefore, better control of processes, has contributed to the success in this area. The especially narrow gap-filling capability of CVD has enabled significant improvement in isolation and interconnect design.

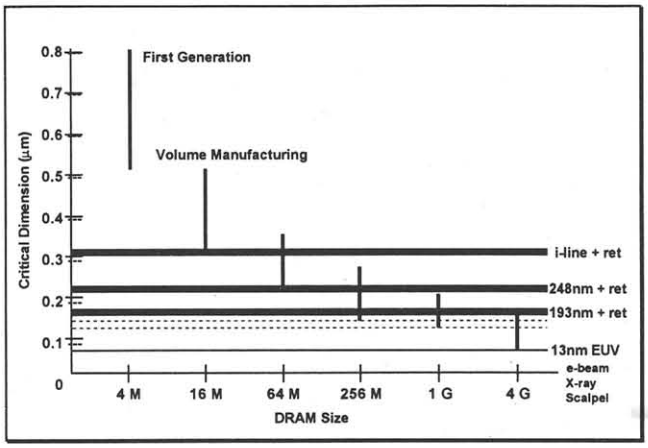

Fig. 2 Lithography Generations

Manufacturing science, including surface control and manipulation has shown its importance through continuous improvement in defect and contamination control[9]. Environmental implications from IC processing has become an increasingly serious concern, prompting a variety of research in terms of the development of environmentally more benign materials and processes, water recycling, etc.; although this discussion is not within the scope of this paper.

4. Summary

Progress and major issues for silicon-based IC technology were discussed by looking into the forthcoming era of sub-0.1μm minimum feature size.

The importance of the need for drastic improvement for on-chip interconnect was emphasized as well as the opportunity and candidates for sub-0.1μm lithography. Although it was not mentioned, the lack of design productivity improvement matching the rate of progress in IC fabrication technology must be remembered. This may severely limit the rate of progress toward the system on a chip.

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