# High Performance n/p Junction Characteristics Using High Temperature RTA in Conjunction with H2 Treatment

## S. Miyazaki, K. Hamada, and T. Kitano ULSI Device Development Laboratories, NEC Corporation 1120 Shimokuzawa, Sagamihara, Kanagawa 229-1198, Japan Phone: +81-427-71-0755, Fax: +81-427-71-0938, E-mail: miya@lsi.nec.co.jp

### **1. Introduction**

Retention time degradation is becoming a serious problem in 64-Mbit DRAMs (Dynamic Random-Access Memories) and will be even more as a problem in future high-density DRAMs [1]. A generation current at the interface trapped state of the LOCOS (LOCal Oxidation of Silicon)/Si is one of the majority origins of the retention time degradation [2][3]. Improvement of SiO<sub>2</sub>/Si interfaces is one of the key issues for both 64-Mbit DRAMs with LOCOS isolation and future DRAMs with STI (Shallow Trench Isolation). It has been reported that hydrogen and fluoride are effective for the reduction of leakage currents, due to the decrease in the interface trapped state [3][4].

In this paper, we reveal that a new electrically active defects, with the exception of the interface trapped states, exists in the peripheral region and is reduced using RTA (Rapid Thermal Annealing) in conjunction with  $H_2$  treatment. The mechanism of the leakage current reduction will also be discussed from the view points of electrically active defects introduced during the LOCOS formation and the interface trapped states at the LOCOS/Si interfaces.

#### 2. Experimental

Figure 1 shows the schematic process flow of the sample fabrication. A p-type well and LOCOS were formed on an epitaxial wafer. Then, a channel stopping layer (guard ring boron) was fabricated just beneath the LOCOS. The n-type diffusion layer was formed by implanting phosphorous. RTA was performed at 1050°C for 30 sec in N<sub>2</sub> ambient after the electrode formation of the phosphorous-doped poly-Si. Finally, H<sub>2</sub> treatment (H<sub>2</sub> sintering) was carried out at a low temperature. Four types of samples (*H*, *HR*, *N*, and *R*) were made with the combination of RTA and H<sub>2</sub>. To make the origin of the leakage current degradation clear, RTA was carried out at 1050°C and 1150°C for 30 sec just before the guard-ring boron implantation (Sample *B10* and *B11*).

We measured the current-voltage (I-V) and capacitancevoltage (C-V) characteristics under reverse-biased conditions. The measured area and perimeter were, respectively, 0.25 mm<sup>2</sup> and 200 mm.

## 3. Results and Discussion

Figure 2 shows reverse *I-V* characteristics for four samples (*H*, *HR*, *N*, and *R*), where the junction leakage current is mainly dominated by a perimeter component. The H<sub>2</sub> treatment (sample *H*, *HR*) is effective in reducing the leakage current. It has been reported that H<sub>2</sub> treatment plays a role in the passivation of the interface trapped state at the LOCOS/Si [4]. The result, thus, means that the leakage current for the sample without H<sub>2</sub> treatment is mainly due to the LOCOS/Si interface trapped state.

The RTA reduces the leakage current for the sample with  $H_2$  treatment. On the other hand, for the sample without  $H_2$  treatment the leakage current increases. These results indicate that the effect of RTA on leakage currents is different for the samples with and without  $H_2$  treatment.

Figure 3 shows n/p junction capacitance at a 3 V reversebias voltage, in addition to the junction leakage current at a 3 V reverse-bias voltage shown in Fig. 2. In this figure, the large 1/C value means there is a wide depletion layer width. The depletion layer width increases after RTA, but is not changed after  $H_2$  treatment. The depletion layer width extended as a result that the redistribution of impurity such as guard ring boron and/or phosphorous in the junction peripheral region takes place after RTA.

In the case of the sample without  $H_2$  treatment, the leakage current increases by RTA, as shown in Fig. 4 [11]. In this case, the dominant component of the leakage currents is the generation current of the LOCOS/Si interface trapped state. Therefore, the density of the interface trapped state is extremely increased by the extension of the depletion layer widths, and the junction leakage current increases.

In contrast, for the sample with  $H_2$  treatment, the leakage current decreases after RTA in spite of the extension of the depletion layer width. This result reveals that the electrically active defect, which can not be passivated by  $H_2$ treatment, exists in the peripheral regions and is reduced by RTA. The influence of the electrically active defect can be observed by reducing generation leakage currents (Fig. 4 [D1]) due to the interface trapped state. Thus, the leakage current is effectively reduced by RTA in conjunction with  $H_2$ treatment (Fig. 4 [D2]).

To investigate the electrically active defect, RTA was carried out at  $1050^{\circ}C$  (sample B10) and  $1150^{\circ}C$  (sample B11) just before the guard-ring boron implantation. Figure 4 shows the junction leakage currents and junction capacitance. The leakage current decreases with the increase in RTA temperature, however, the depletion layer width, that is the impurity profile, is not changed. These results indicate that electrically active defects introduced during the LOCOS formation are annihilated by RTA, and that the leakage current subsequently reduced.

## 4. Conclusions

We demonstrated the existence of the electrically active defect induced during LOCOS formation and the reduction of this electrically active defect by RTA. The influence of the electrical active defect can be observed by reducing the leakage currents which are due to the decrease in the interface trapped state by  $H_2$  treatment. As a result, RTA by itself and RTA in conjunction with  $H_2$  treatment effectively reduce the leakage current.

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Fig. 2. Reverse I-V characteristics for H, HR, N, and R.

