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Quantitative Evaluation of Dopant Loss in Low Energy As Implantation for Low-Resistive, Ultra Shallow Source/Drain Formation

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Abstract

The dopant loss in 5-10 keV As ion implantation for sub-0.1 μm MOSFET source/drain formation has been quantitatively investigated. When implantation energy is lowered to 5 keV, 43 % of implanted As remain in a 5 nm screen oxide. Moreover 50-70 % of As in Si are lost by dopant pileup at the SiO_2/Si interface during 850 °C annealing. Thus the pileup problem becomes severer with junction depth reduction. By optimizing the screen oxide thickness, the implantation energy and the ion dose, both low sheet resistance and ultra shallow junction depth have been simultaneously achieved.

1. Introduction

For MOSFET scaling ion implantation energy should be lowered to form shallower source and drain (S/D) junctions. Successful fabrication of sub-0.1 μm MOSFETs using low energy (2-5 keV) As implantation has been reported[1-2], while the details of low energy As implantation have not been discussed in terms of the profile, junction depth and sheet resistance. In a previous paper we have reported drastic increase in the sheet resistance due to As ion energy reduction down to 5 keV[3]. This paper describes the origin of the sheet resistance increase in 5-10 keV As ion implantation based on dopant loss mechanisms.

2. Experimental

Figure 1 shows the schematic process flow of junction formation and evaluation. Arsenic ions were implanted into p-type Si(100) substrates with or without a 2.5-5 nm screen oxide at a dose of 1×10^{14}-1×10^{15} cm^{-2}. Furnace annealing(FA) was performed at 850 °C in N_2 for 30 min. The amount of retained As and the junction depth X_j were evaluated by SIMS analysis.

3. Results and Discussion

In practical MOS device fabrication, dopant ions are implanted through the screen oxide to prevent metal contaminations and gate oxide damage. Since the projected range for As in SiO_2 is about 7 nm at 5 keV[4], considerable amount of As remains in a screen oxide with a thickness of more than a few nm. Thus dopant loss due to screen oxide γ_s which is defined by the ratio of the amount of As incorporated in SiO_2 to the total implanted As was measured by changing implantation energy and screen oxide thickness as shown in Fig. 2. About 43 % of implanted As are incorporated in a 5 nm screen oxide for 5 keV implantation.

Severe dopant loss is induced by As pileup in the vicinity of the SiO_2/Si interface during the furnace annealing as shown in Fig. 3. Most part of pileup As is removed with oxide stripping by 0.5 % HF. Figure 4 shows the SIMS profiles after HF dipping for wafers implanted through a 5 nm screen oxide with a dose of 1×10^{14} cm^{-2}. The As peaks are reduced to 2-4$\times10^{19}$ cm^{-3} after oxide stripping regardless implantation energy. The pileup ratio γ_p as defined by the ratio of As loss by pileup after annealing to the amount of implanted As in Si is larger than 48 % and increases as the implantation energy becomes lower(Fig. 5). Nishida et al.[5] have reported that the carrier activation is deteriorated as the energy of As ion implantation is lowered and the reason is not clear. They have defined the activation efficiency as the sheet carrier concentration divided by implanted As in Si before annealing. We consider that the increase of γ_p due to ion energy reduction apparently degrades the activation efficiency. To understand the energy dependence of γ_p the extent of As pileup for different annealing times was measured as shown in Fig. 6. During the first 5 min, the pileup layer is already formed and the profile remains almost unchanged in the interface even by further annealing. Aoki et al.[6] also have shown that the As pileup region remains even for a long annealing time, namely, pileup As is immobile during annealing. The As distribution peak approaches the SiO_2/Si interface with decreasing implantation energy, and hence the amount of As which can reach the interface for pileup increases. It is likely that almost all pileup As atoms are transported during the solid phase regrowth at a quite early stage as understood from Fig. 6. Figure 7 shows the total dopant loss γ_{total} as determined by $\gamma_s+(1-\gamma_s)\gamma_p$ versus implantation energy. The value of γ_{total} increases as the implantation energy is lowered because of the energy dependence of both γ_s and γ_p.

The energy lowering to make junction shallower results in the severe dopant loss as described above. Low energy As implantation for sub-0.1 μm MOSFETs can be optimized by trade-off between the sheet resistance R_s and the junction depth X_j. Figure 8 shows the relation between R_s and X_j under various energy and dose conditions. At a dose of 1×10^{14} cm^{-2}, R_s steeply increases as energy is lowered to 5 keV(the top dash line in the figure) because of the enhanced dopant loss. However, by compensating the dopant loss with increasing the ion dose, R_s can be reduced down to 0.8 kΩ/sq. even at 5 keV. The difference in X_j due to increasing ion dose from 1×10^{14} to 1×10^{15} cm^{-2} is 10 nm for 5 keV. Thus, low R_s and shallow X_j can be simultaneously obtained by selecting a high dose for low energy As implantation.

4. Summary

We have investigated the dopant loss in low energy As implantation. When the implantation energy is reduced to 5 keV, the significant portion of As is lost due to incorporation in the screen oxide and the dopant pileup at the SiO_2/Si interface. Pileup becomes severer as the As peak becomes closer to the interface. We found that the pileup proceeds at a quite early stage of annealing. A possible direction to obtain shallow junctions with low sheet resistance has been proposed.

Acknowledgements

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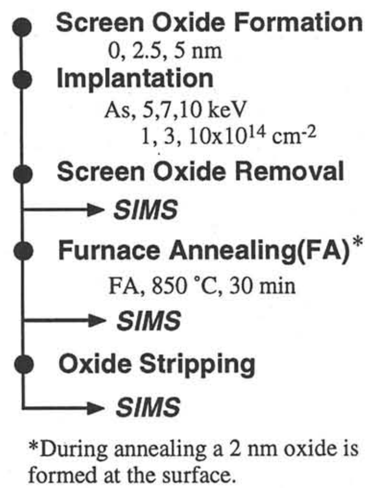

Fig. 1 Junction fabrication process flow.

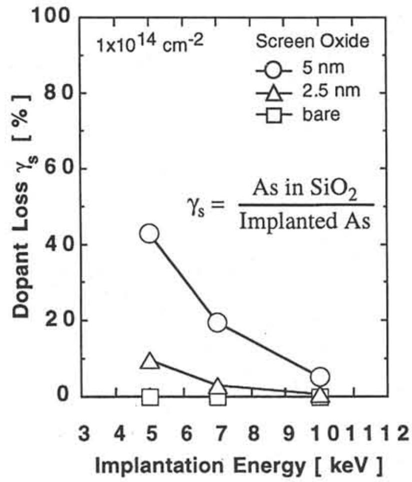

Fig. 2 Arsenic loss due to screen oxide γ_s against implantation energy.

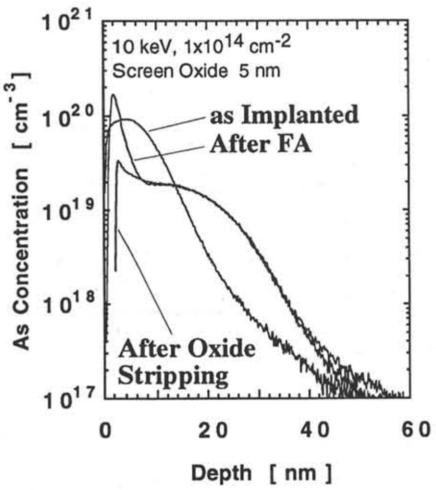

Fig. 3 SIMS depth profiles before and after annealing.

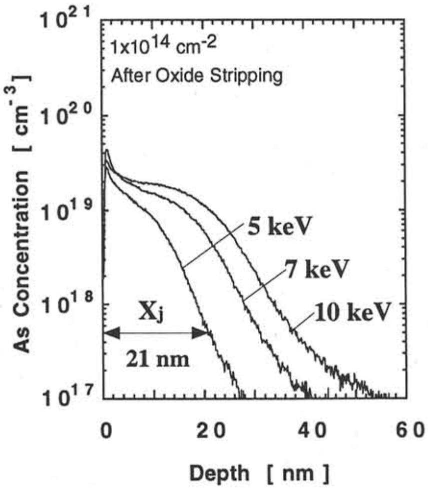

Fig. 4 SIMS depth profiles after removal of pileup region by HF dipping. The junction depth is defined as a depth where As concentration is 5×10^{17} cm^{-3}.

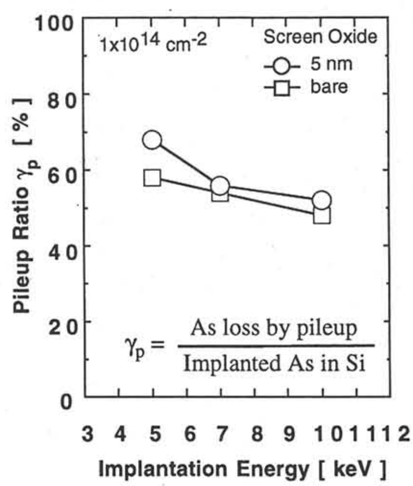

Fig. 5 Pileup ratio γ_p against implantation energy. Value of γ_p becomes larger as the implantation energy is lowered.

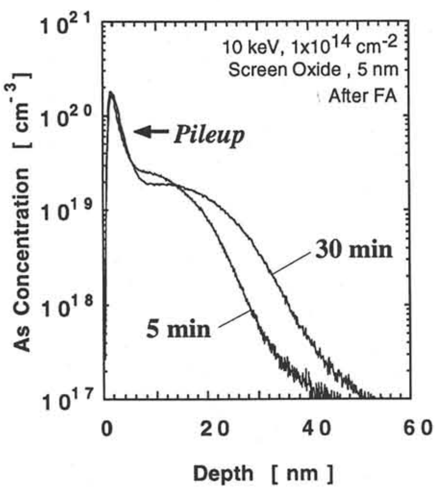

Fig. 6 SIMS depth profiles for different annealing times.

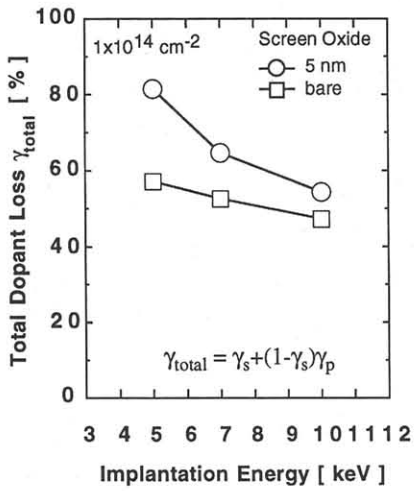

Fig. 7 Total dopant loss γ_{total} against implantation energy.

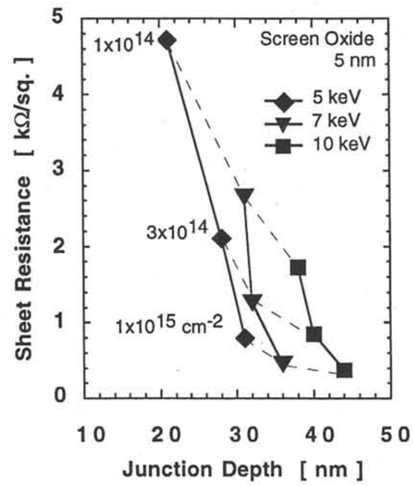

Fig. 8 Relationship between sheet resistance and junction depth.