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Ultrathin Nitride/Oxide (N/O) Gate Dielectrics for p$^+$-poly Gated PMOSFETs Prepared by a Combined Remote Plasma Enhanced CVD/Thermal Oxidation Process

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1. Introduction

As the aggressive scaling of CMOS devices continues, nitride/oxide dual layer gate dielectrics have become promising candidates as alternatives to thermal oxide gate dielectrics in dual gate FETs. One of their advantages is the ability of the nitride layer to act as a boron (B) diffusion barrier. We have previously shown that 0.8 nm of plasma-deposited nitride is able to suppress B-atom transport of p+ gates during a high thermal budget dopant activation [1]. At this thickness the product the areal density of N-atoms and their effective area is approximately 1.0, so that interactions between B-atoms and O-atoms of the underlying oxide layer are blocked. High temperature nitridation of thermal oxides has also been used to suppress boron diffusion. However, because the N-atom concentration is peaked at oxide/substrate interface, this results in boron accumulation in the bulk oxide, degrading oxide reliability [2]. With the diffusion barrier placed at poly-silicon/oxide interface, the N/O dual layer dielectrics have shown improved reliability by preventing boron diffusion into oxide layer [1]. In addition, because silicon nitride provides almost twice the dielectric constant of silicon dioxide, lower tunneling currents in the direct tunneling regime can be obtained for the same equivalent oxide thickness [3].

In this work, we have investigated the characteristics of p+-poly gate PMOSFETs with N/O dual layer gate dielectrics. The nitride layers were prepared by remote plasma enhanced chemical vapor deposition (RPECVD) and the oxide layers by thermal oxidation. It is shown below that these N/O dielectrics suppress of boron diffusion out of the gate electrode, thereby eliminating some short channel effects while maintaining excellent oxide reliability and interface properties. In addition, improved immunity against hot carrier stressing was observed for N/O dielectrics compared to single layer oxides.

2. Experimental

PMOSFETs, without LLD drains, but with p+-poly gates and L/W = 0.8μm/20μm were fabricated on 1~10 ohm-cm n-type Si<100> substrates. Channel doping was increased to ~ 6.7 x 10^{17}/cm^3 by phosphorus implantation. A 2.6nm oxide was grown in dry oxygen at 800°C. This was followed RPECVD deposition of a 1.5nm nitride using SiH_4 and N_2 as source gases [4]. The nitride thickness was estimated from the deposition rate, and *confirmed* to ± 0.1 nm by Auger electron spectroscopy [5] and ellipsometry. Post-deposition annealing of the dual layer was performed in He at 900°C for 30 s to reduce the hydrogen concentration in plasma deposited nitride [6]. Polysilicon was deposited, implanted with boron (20keV, 5×10^{15}/cm^2), and then the boron was activated at 950°C for 60 s. An equivalent oxide electrical thickness (T_{ox-eq}) of 3.5nm was obtained from analysis of high-frequency C-V data.

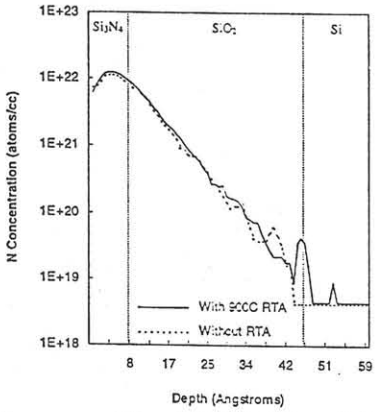

Fig. 1 Nitrogen profile of N/O (~0.8nm/4.0nm) dual layer gate dielectrics with and without RTA at 900°C for 30sec.

3. Results and Discussion

Figure 1 shows nitrogen SIMS profiles for N/O ~ 0.8nm/4.0nm dielectrics including the effect of post-deposition annealing. The plasma deposited nitride film is clearly evident. The *trailing* of nitrogen into the oxide is an artifact of the SIMS process. After annealing at 900°C for 30sec, a nitrogen peak appears at the oxide/silicon interface, showing that N-atoms diffuse into, and pile up at the oxide/silicon interface during the anneal. The Si-N bonds at the interface replace Si-O bonds, relieving interface strain to the smaller effective size of the nitrogen atoms, and additionally provide a smoother interface [7], Suppression of boron diffusion from the gate electrode has been monitored by C-V and Id-Vg characteristics. As shown in Fig. 2, both C-V and Id-Vg traces are shifted to more positive voltages for the thermal oxide device, indicating a significant penetration of boron to the Si channel. This demonstrates that the top nitride layer in N/O structure is effective in suppressing boron diffusion out of the gate electrode. In addition, because

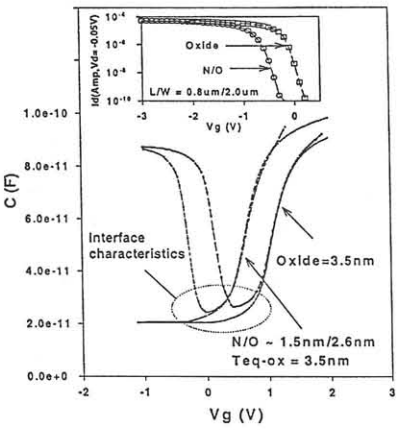

Fig. 2 CV and subthreshold Id-Vg characteristics for N/O and SiO_2 gate dielectrics with boron-implanted polysilicon.

the separation of the high-frequency and quasi-static C-V curves at the onset of inversion is determined by the interface state characteristics, it is clear that N/O dual layer dielectrics has a reduced density of interface defect states. This is assumed to be due to the incorporation of nitrogen at oxide/substrate interface during the post-deposition anneal.

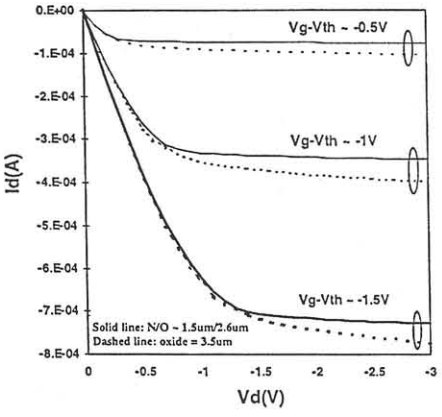

Fig. 3 Id-Vd characteristics of N/O dual layer (solid) and oxide (dashed) PMOSFET's - channel length 0.8 μm.

Figure 3 shows the Id-Vd characteristics of 0.8μm channel length PMOSFET's for N/O dual layer and single layer oxide gate dielectrics. The N/O dual layer device shows better saturation characteristics than device with the oxide. The increased slope of the Id-Vd curve in the saturation region for the oxide is indicative of an enhanced short channel effect associated with boron penetration. The effective mobility of N/O dual layer and oxide devices were extracted form large transistors (W/L=100um/100um) to avoid the effects of uncertainties in the source/drain series resistance. As shown in Fig. 4, exactly same effective mobilities were obtained for N/O dual layer and oxide devices, indicating an advantage of the low temperature RPECVD process in maintaining the oxide/substrate interface integrity. Also, due to the nitrogen incorporation at oxide/substrate interface during the post-deposition anneal, the PMOSFET with N/O dual layer dielectrics shows a reduced ΔG_m during hot carrier stressing, implying a more robust Si/SiO_2 interface. This improved interface immunity against hot carrier stress is believed to be due to interfacial strain relaxation that occurs for the substitution of interfacial Si-O bonds by Si-N bonds [8].

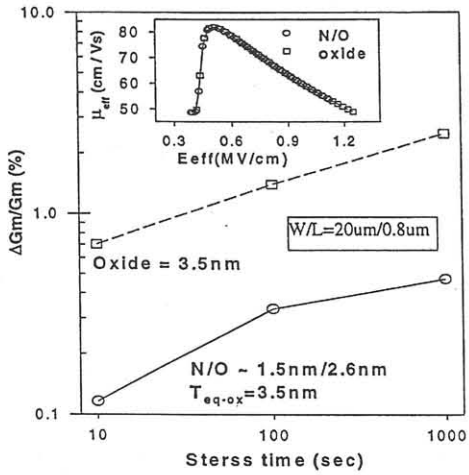

Fig. 4 Stress-time dependence of Gm degradation (Vg-Vth = -2.1V, Vd = -7.5V) and effective hole mobility verses effective normal field of PMOSFETs.

4. Conclusions

N/O dual layer gate dielectrics prepared by an RPECVD/oxidation process with equivalent oxide thickness of 3.5nm have been fabricated for p+-poly PMOSFETs. The nitride layer reduces boron penetration into the oxide and channel, thereby eliminated some short channel effects, and improving hot carrier stress degradation. Since they maintain the same effective mobility as oxide devices and improve reliability, the N/O dual layer gate dielectrics show good promise for sub-0.25 μm dual-gate CMOS technology.

Acknowledgments

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