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Dual Gate Oxide Process Integration for High Performance Embedded Memory Products

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1. Introduction

A high performance logic circuit with embedded memory devices needs two thicknesses of gate oxide. One is a thin gate oxide for the logic MOSFET and the another one is a thick gate oxide for the memory device and/or the high voltage transistor. These gate oxide films are integrated on a wafer through Dual Gate Oxide (DGO) process. This DGO process is required to retain logic MOSFET performance and to meet memory device characteristics (i.e. low leakage, proper active point, etc). For the requirements, some DGO process integrations has been proposed on the logic process platform. In this study, a DGO process was realized for 40Å-gate/90Å-gate with common well dopings on a wafer. The electrical measurement results are shown comparing the DGO wafers to the single gate oxide wafers. The manufacturability issues of each DGO process are also discussed.

2. Processing

Some experimental wafers were processed to make a single gate oxide condition (40Å or 90Å) and to realize the DGO conditions (40Å/90Å). The process flow schematic diagram is shown in Fig 1. After Trench isolation, the well and Vt adjust implants were the same condition as 40Å logic baseline process. The single gate oxide wafers were oxidized only once for each gate oxide thickness (40Å or 90Å). The DGO process were tried two ways. The one was Thick-Thin (TTDGO) process that the wafer was oxidized for 90Å gate at first, the 90Å oxide was removed from thin gate part, and the wafer was oxidized again for 40Å gate. The other was Thin-Thick (DGODP) process that the wafer was oxidized for 40Å gate at first, followed by 1st poly-Si deposition, the 1st poly-Si and 40Å oxide was removed from thick gate part, and the wafer was oxidized again for 90Å gate and the 2nd poly-Si was deposited. The excess 2nd poly-Si was etched from 1st poly-Si. Following the gate poly photo, all wafers took same process flow as the logic baseline.

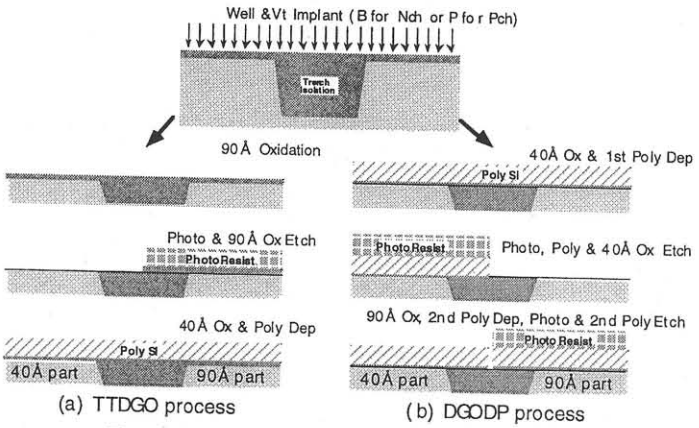

Fig 1. Experimental process flow diagram

3. Experimental Results

3-1. Qbd

Fig 2 shows Weibull plots of the Qbd measurement result for 40Å-Gate oxide and 90Å-Gate oxide. In Gate Injection condition, both DGO wafers had almost same distribution on the Weibull plots as Single-Gate wafers. In Substrate Injection condition as the opposite direction, the Qbd on DGODP wafers was a little bit degraded than Single-Gate wafers for 90Å. It seems be a field edge effect from excess trench oxide recess. In spite of this, the oxide qualities are still acceptable for actual device's reliability.

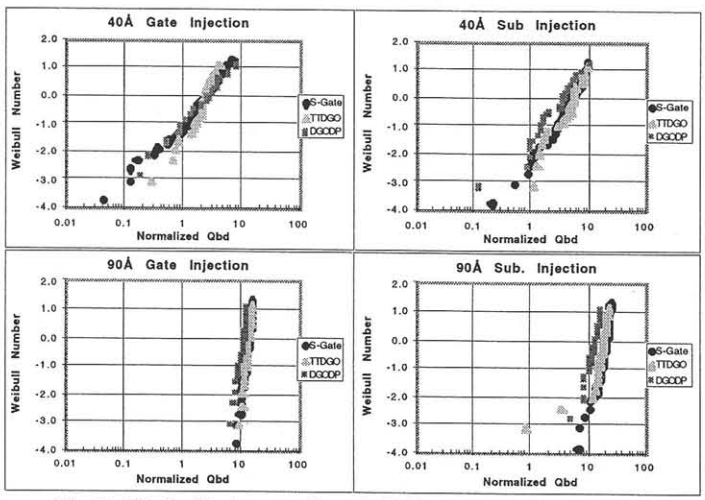

Fig 2. Weibull plot graphs of Qbd measurement results

3-2. MOSFET characteristics

Fig 3 shows composite ID-VG graphs of a large size MOSFET (W/L=18μm/18μm) on the Single-Gate wafers and on the DGO wafers. The Vt(Sat) roll-off graphs are shown in Fig 4.

For 40Å-Gate MOSFETs, the characteristics were almost same on both the Single-Gate and the DGODP conditions. Vt (linear) shifts of the large size MOSFET on the DGODP wafer were only -22mV as decrease direction for Nch and -28mV as increase direction for Pch from Single-Gate condition. These

shifts were caused by an additional thermal budget and impurity re-distribution as the 90Å-Gate oxidation. However, the TTDGO condition's wafer had large Vt shift (0.1~0.14V) as decrease direction on both Nch and Pch. These Vt shifts were caused by impurity segregation during the former 90Å gate oxidation as the simulation result shown in Fig 5. Such the Vt shift is serious problem for the short channel 40Å MOSFETs.

For 90Å-MOSFETs, the TTDGO wafer had almost same characteristics as Single-90Å wafer. In opposite way, the DGODP wafer had large Vt shift that were -100mV as decrease direction for Nch and +84mV as decrease direction for Pch. These Vt shifts also were provided by an impurity segregation during the preceding 40Å-Gate oxidation as mentioned above. However, the Vt shift resulted in the proper Vt for the circuits, and further, the Vt decrease brought higher drive current density than just Single 90Å-Gate MOSFETs.

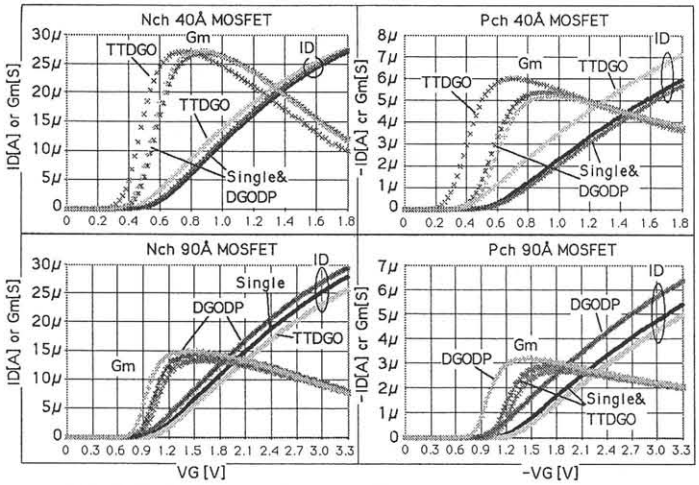

Fig 3. MOSFET characteristics (W/L=18μm/18μm)

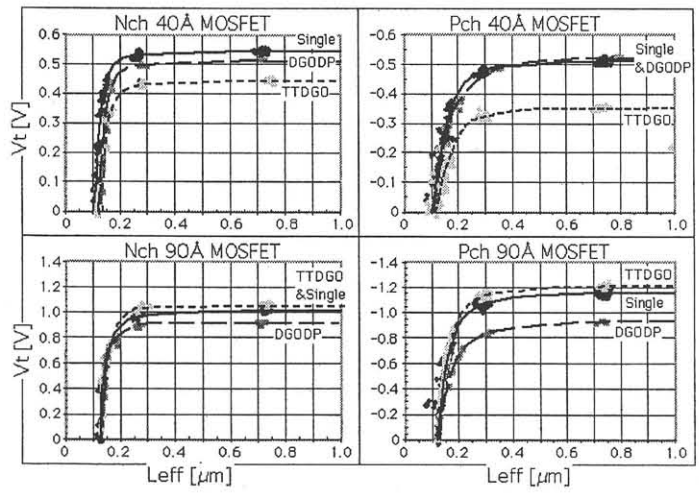

Fig 4. Vt(Sat) roll-off characteristics

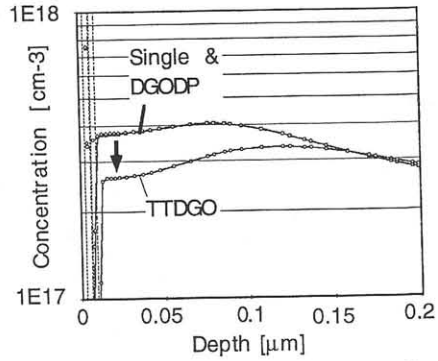

Fig 5. A simulation result of Net concentration profile

Table 1. Gate oxide and MOSFET comparison summary

	Single		TTDGO		DGODP	
	40Å	90Å	40Å	90Å	40Å	90Å
QBD	◎	◎	◎	○	◎	○
Nch Vt	—	↑	↓	↑	—	↓
Pch Vt	—	↑	↓	↑	—	↓

4. Discussion

4-1. Vt adjustment

On TTDGO process, a 50%-increase in the Vt adjust dosage was tried in order to recover the 40Å MOSFET's Vt. However, this trial resulted in a recovery of 60~70mV only, while the Vt of the 90Å MOSFETs was increased by 0.2~0.3V. It is hard to compansate such the segregation impurity loss is very hard to be compensated. If a dopant with lower-segregation-factor such as In and Sb were used instead of B and P, it should be easy to fix the Vt shifts. However in that case, the Vt adjustment for 90Å MOSFETs will be separated from 40Å MOSFETs

5. Conclusion

The DGODP process is one solution of the integrations for Embedded Memory products on the current logic baseline. In this process, we have demonstrated same gate oxide quality, retaining of 40Å MOSFETs and proper 90Å MOSFETs using same Well & Vt adjustment conditions as logic baseline process. The remaining issue is HCI life time improvement for thick gate devices.

6. Acknowledgements

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7. References

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