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The Deuterium Effect on SILC

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1. Introduction

Lyding, Hess, and Kizilyalli have recently reported that in place of H_2 with D_2, transistor lifetime for a 10% reduction in the transconductance is enhanced by factors of 10~50 [1]-[2]. This is because the energies involved in chemical bonding are the same for both isotopes, but the vibration frequency of D-Si bond is close to phonon frequency of Si lattice. Consequently, under hot electron stress, the energy to D-Si bond can be easily transferred to Si-atom vibration. However, the above improvement study is focused only on Si and oxide interface. Because the Si dangling bonds exist in both interface and Si-oxide transition region that behave as Q_{it} and Q_f charges in oxide, it is also interesting to study the D_2 effect on the bulk-oxide. In this work, we have analyzed the D_2-annealing effect on SILC, and direct comparison with H_2-annealing is also presented. It is found that D_2-annealing have little effect on thick 70-Å oxide, under our stress condition. In contrast, significant improvement was observed on ultra-thin 27-Å oxide while SiO_x transition region and a high concentration of dangling bond dominate most part of this direct tunneling oxide.

2. Experimental

The (100) orientation, 14~17Ω-cm resistivity, p-type Si wafer was used in this study. After a modified RCA cleaning, thermal oxide of 27 and 70-Å were grown at a temperature of 900 °C. The thick 70-Å oxide was grown in a conventional furnace, while the thin 27-Å oxide was grown in a leak-tight furnace that has the capability of *in-situ* desorbing the native oxide. After standard MOS capacitor fabrication, some samples were annealed at 400 to 425 °C for 30min. The annealing is performed in pure H_2 or D_2 ambient under a leak-tight low-pressure furnace. SIMS was used to study the D_2 incorporation process, and capacitor I-V and SILC evaluated the electrical characteristics.

3. Results and Discussion

Figs. 1(a) and 1(b) show the SIMS profiles with D_2 annealing after different process-step of oxide and poly-Si, respectively. As shown in Fig. 1(a), there is an accumulation of mass-2 at the oxide and Si-bulk interface. Because the mass-2 signal may be from single-charged H_2, it is difficult to conclude that this signal is related to D-atoms; especially there is also a strong H_2 atom accumulation at the same position. On the other hand, the D_2-annealed sample after poly-Si process (Fig. 1(b)) shows that a strong accumulation also occurs at poly-Si surface and is gradually diffused into oxide. Because the only difference between these two data is the different annealing step, therefore the accumulation of mass-2 signal is due to D_2-annealing and the mass-2 signal is mainly from D-atom. The reason why D_2 accumulation at poly-Si may be due to the existing large amount of dangling bonds in grain boundaries.

We have further studied the SILC effect on D_2-annealed oxide. Figs. 2(a), and 2(b) show the comparison of H_2- and D_2-annealed MOS capacitors respectively, and the oxide thickness is 70-Å. The stress is performed under a current density of 0.1A/cm^2 and total injected charges for 2 Coul/cm^2. Although typical SILC effect is observed from Fig. 2, there is almost no difference between these samples. Therefore the D_2-annealing effect on thick 70-Å oxide has no improvement of reliability as compared to H_2-annealing, under our stress condition.

We have also studied the D_2-annealing effect on thin gate oxides. Fig. 3(a) shows the annealing effect on SILC, and the measured I-V curves show typical direct tunneling characteristics. Owing to the large tunneling current, the stress is performed at a high current density of 16.5A/cm^2. Because the SILC effect is relatively small in direct-tunneling oxide, we have plotted the change of tunneling current in Fig. 3(b). In sharp contrast to thick oxide, near an order of magnitude improvement is observed in D_2-annealed sample to H_2-annealing. This large difference may be due to the presence of large amount of defects in ultra-thin oxide. Actually, it is reported recently by C. T. Liu *et al* from Bell Labs at IEDM that an intrinsic defect may exist in thin gate oxide, and such defect will increase the leakage current that is similar to SILC. Therefore the large improvement of SILC may be due to this intrinsic defect passivation.

To further view this intrinsic defect microscopically, we have plotted the possible bonding structure in Fig. 4. The microscopic picture of thick oxide contains both SiO_2 and transition SiO_x (x:0-2). However, most part of this ultra-thin 27-Å oxide is in the SiO_x transition region where high concentration of unsaturated bonds exists. This unsaturated bonds in transition region is similar to that in oxide and Si interface, where both cases contribute positive charges Q_f and Q_{it} to oxide. Therefore the D_2 may play the same role in both transition SiO_x and interface.

4. Conclusion

In conclusion, we have studied the D_2-annealing effect on thermal oxides. Significant improvement can be observed in direct tunneling oxide that is due to passivation of intrinsic defect and dangling bonds in transition SiO_x layer.

References

1. J. Lyding, K. Hess, and I. Kizilyalli, Appl. Phys. Lett. 68, (1996) 2526.
2. I. Kizilyalli, K. Lyding, and K. Hess, IEEE Electron Device Lett. 18, (1997) 81.

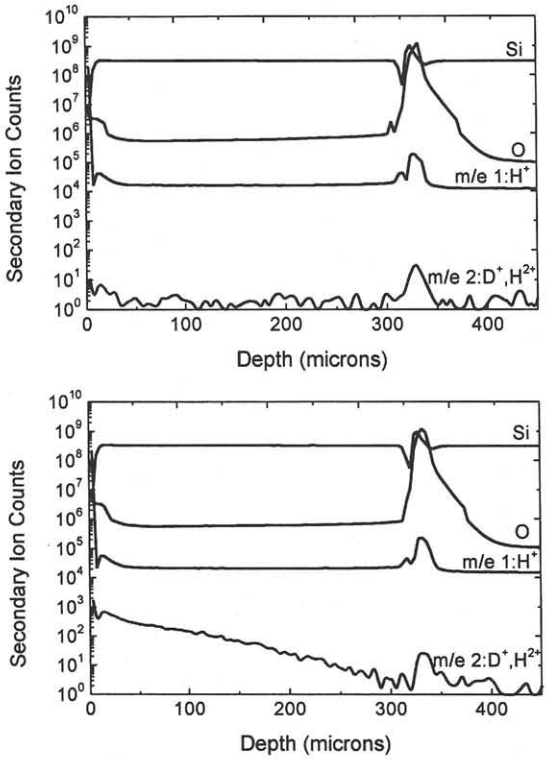

Fig. 1. SIMS profile of 3000Å poly-Si/70Å oxide/Si structure. The D_2-annealing is performed (a) after oxide growth or (b) after poly-Si.

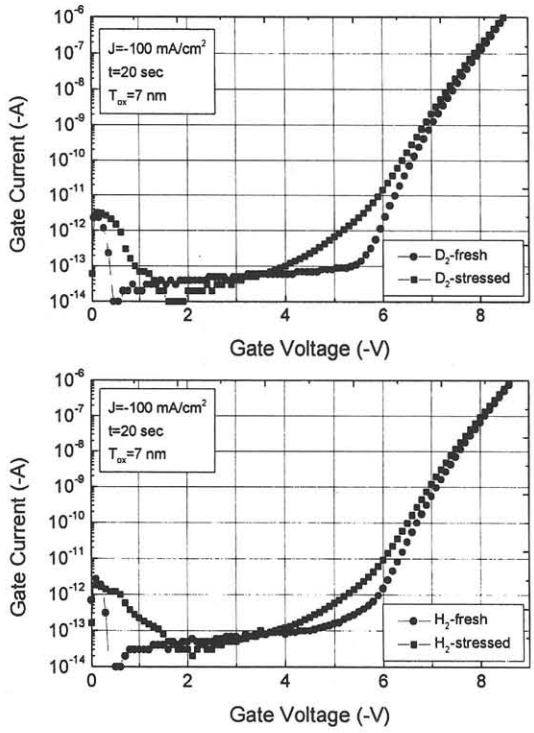

Fig. 2. Stress effect of (a) H_2- and (b) D_2-annealed MOS capacitors. The oxide thickness is 70-Å.

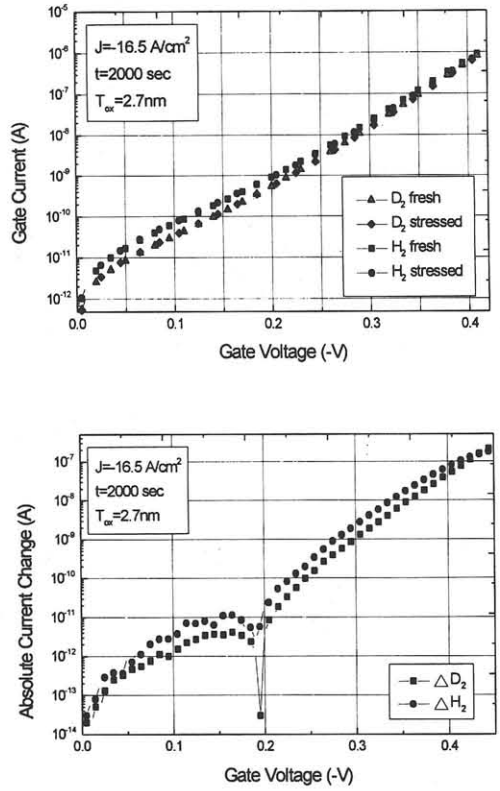

Fig. 3. Stress effect of (a) H_2- and (b) D_2-annealed MOS capacitors. The oxide thickness is 27-Å.

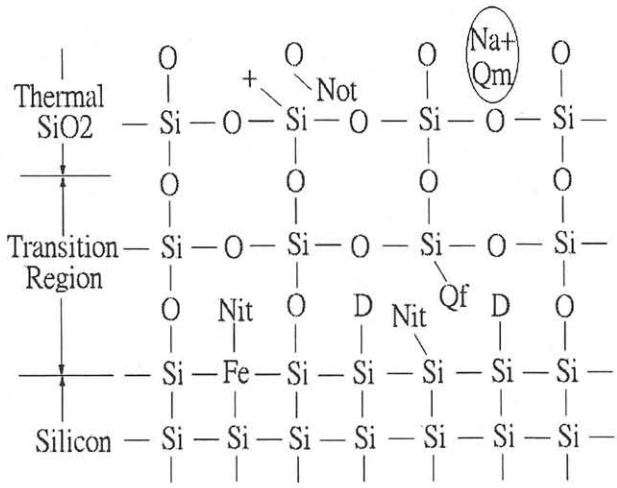

Fig. 4. Microscopic picture of thermal oxide