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Differences between the Electrical Properties of Nitrided Si-SiO_2 Interfaces Formed by (a) Post-Oxidation, Remote Plasma-Assisted Nitridation and (b) Remote Plasma-Assisted Deposition

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1. Introduction

Interface nitridation of ultrathin gate oxides promotes increased reliability in nmos devices without sacrificing device performance. However, interfacial nitridation of pmos devices requires additional top surface nitridation to block boron transport out of p+ polycrystalline silicon gate electrodes for oxide thicknesses <4 nm. Interface nitridation has been performed by several different methods [1]: i) high-temperature nitridation of thermally-grown oxides in ammonia (NH_4), nitrous oxide (N_2O), or nitric oxide (NO) gasses, (ii) high-temperature thermal oxidation/nitridation of silicon surfaces in N_2O or NO, and (iii) low-temperature plasma-assisted oxidation using N_2O [2]. Optimized interface concentrations of N-atoms are of the order of one monolayer.

An alternative approach to interface nitridation is given in this paper in which oxide thickness and nitridation are separately and independently controlled in a low-temperature, low-thermal-budget two-step process: O_2 plasma oxidation of Si is followed by N_2 plasma nitridation to incorporate N-atoms at the Si-SiO_2 interface. This post-oxidation, interface nitridation process is compared with deposition of ultrathin silicon nitride layers onto H-terminated silicon surfaces.

2. Experimental Procedures

The processing for incorporation of nitrogen at Si-SiO_2 interfaces includes two 300°C steps: (i) remote plasma-assisted oxidation (200 sccm He/20 sccm O_2) to form a superficial oxide layer, ~0.5-0.6 nm thick, and (ii) remotely activated N_2/He plasma nitridation (160 sccm He/60 sccm N_2) to incorporate nitrogen at the Si-SiO_2 interface. Both processes are performed at a pressure of 0.3 Torr and an RF power of 30 W. N-atom incorporation at the interface is controlled by varying the N_2 plasma exposure time. For the bulk SiO_2 deposition, remote plasma enhanced chemical vapor deposition (RPECVD) with plasma-excited He/O_2 and downstream injected SiH_4 was employed. Rapid thermal annealing was performed in He at 0.3 Torr at 900°C for 30 s in an on-line RTA chamber. Nmos and pmos capacitors were made using conventional processing and photolithography. On-line AES was performed in an on-line analytical chamber to study nitridation, and SIMS was done at EVANS EAST.

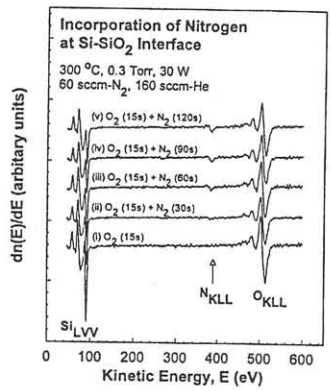

Fig. 1. Differential AES for nitrided interfaces.

3. Interface characterization and metrology

Interfacial confinement of N-atoms was confirmed using on-line AES to monitor N-atom features as a function of exposure time to the N_2/He plasma. Figure 1 gives on-line AES data after: (i) a 15 s O_2 plasma exposure which grows a ~0.5-0.6 nm thick superficial oxide, followed by N_2/He plasma nitridation for (ii) 30 s, (iii) 60 s, (iv) 90 s, and (v) 120 s. The intensity of nitrogen KLL peak at ~375 eV increases with increasing exposure time showing that longer exposures result in increasing nitrogen incorporation. The ratio of the N_{KLL} to the Si substrate LVV peak is linear in time demonstrating that the N_{KLL} signal suffers the same attenuation as the Si substrate feature. so that N-atoms are at the Si-SiO_2 interface. rather than *in, or on top of* the oxide.

The nitrogen content was quantified by secondary ion mass spectroscopy (SIMS) using both CsN^+ and SiN^- ions. Integration of SIMS depth profiles indicates that interfacial nitrogen content varies linearly with nitrogen exposure time. A comparison of the SIMS data taken in this experiment with data of Ref. 2 indicates approximately one monolayer is results from an exposure time of about 90 s.

4. Results of Electrical Measurements

In experiments performed on both nmos (substrate injection) and pmos (gate injection) devices with 5 nm thick

oxide s and Al gate metal electrodes, it was shown that the Fowler-Nordheim (F-N) tunneling current at a fixed voltage decreased with increasing nitridation (see Fig. 2). CV measurements indicated that the flatband voltages varied by less than 0.05 V, so that these large reductions in current are not due to built-in potentials associated with fixed or trapped charge that accompanies the plasma interface nitridation.

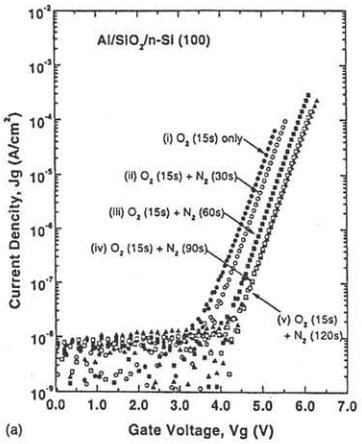

Fig. 2. J-V characteristics for nmos capacitors.

Similar results have also been obtained in the direct tunneling regime for nmos and pmos devices with thinner oxides (~2 to 3 nm). These devices had poly-Si gate electrodes, phosphorus-doped for the n+ poly-Si, and boron-doped for the p+. It was necessary to use either a top surface nitridation process [3,4], or nitride layer [5] to suppress boron out-diffusion from the p+ poly-Si gate. These experiments, like those in the F-N regime, demonstrated order of magnitude decreases in tunneling currents that were i) independent of the direction of injection, substrate of gate, ii) independent of the oxide thickness, and therefore the tunneling regime, F-N or direct, and iii) independent of the gate electrode material, n+ poly-Si, p+ poly-Si or Al.

In a final set of experiments, capacitors and FETs with monolayer interface nitridation formed by the plasma-assisted processes discussed above, were compared with interfaces formed by direction deposition of ultrathin silicon nitride. The nitride layers were deposited by RPECVD at 300°C and

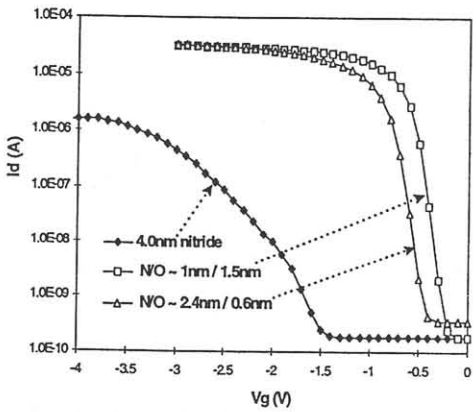

Fig. 3. Id-Vg plots for pmos FETs.

subjected to a 900°C RTA, a sequence that results in device-quality nitrides when incorporated into ONO [6], or NO devices [4,7]. In capacitor and FETs interfaces formed by direct deposition of ultrathin, or thick nitride films, there were significant flatband voltage shifts (> 0.5 V) indicating fixed or trapped positive charge levels of at least 10^{12} cm^{-2}.

Figure 3 shows results obtained for pmos FETs that demonstrate that deposition of a nitride layer directly onto a hydrogenated Si surface produces significant degradation. In previous studies [4], it was shown that the threshold voltage for pmos FETs with ON gate dielectrics was ~ -0.3 V, as for the device with the NO (1 nm/1.5 nm) dual layer gate. Reducing the oxide layer thickness to 0.6 nm resulted in a small shift, ~0.1 eV in the threshold voltage, but does not reduce the drive current for larger applied voltages. The two devices with NO dielectrics and the device with the 4 nm nitride layer have essentially the same oxide-equivalent thickesses, ~ 2 nm, so that equal drive currents are expected. However, the device with the 4 nm nitride shows markedly degraded behavior: i) a large shift of the threshold voltage to more than -1.4 V, ii) more than an order of magnitude reduction in drive current, and iii) a *soft* current turn-on.

5. Conclusions

Significant reductions in tunneling current have been demonstrated for plasma-nitrided Si-SiO_2 interfaces. These reductions can not be assigned to systematic changes in flatband voltages associated with nitrogen generated interfacial defects. It is possible that the current reduction is due to decreased roughness. It was also demonstrated that direct deposition of nitrides onto clean Si surfaces produces significant degradation of interface properties; e.g. shifts in flatband voltages due to fixed or trapped positive charge. This means that defect generation is suppressed by monolayer nitridation, but defects are produced in nitride layers in direct contact with the Si substrate. This is contrast to the absence of charged defects when similarly prepared nitride layers that are incorporated into ONO or ON composite dielectrics.

Acknowledgments

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