Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 258-259

Invited

Copper Interconnects for Advanced Logic and DRAM

James G. Ryan, Gary B. Bronner, John P. Hummel and Thomas N. Theis[1]

IBM Microelectronics, SRDC, Hopewell Jct., NY 12533 and [1]IBM Research, T. J. Watson Research Center, Yorktown Heights, NY 10598

Introduction

The use of advanced interconnect structures featuring low k dielectrics or copper wiring have allowed continued enhancements in integrated circuit (IC) performance. For example, low k dielectrics have been used primarily for logic applications in order to improve performance and lessen power consumption. Copper interconnect technology has also been used in logic products and, more recently, demonstrated for memory applications. It is expected that ICs with the combination of copper wiring and low k intermetal dielectric (IMD) will be available by the 0.13 υm generation. This paper describes the results of an evaluation of copper wiring technology in DRAM products and also discusses the design, materials and process improvements needed to make copper wiring and low k insulators extendible to advanced devices.

Copper Wiring Applications

Copper wiring was evaluated in two DRAM products to understand it's impact on device performance. A 4 Mb DRAM product similar in construction to the product in reference 4 was used as a demonstration vehicle. Copper wiring fabricated by the damascene method was used as the first metal level (M1). Barrier thickness was varied in order to determine if any threshold voltage shifts were apparent due to the use of copper wiring. Table I shows the results of post-fabrication device testing. No significant threshold voltage shifts were observed due to copper. Additional evaluations were performed using a 0.35 υm 64 Mb DRAM. Copper based interconnect was used at the M1 level (Fig. 1). Fabrication details are described in reference 2. Retention time and junction leakage were unaffected by the presence of copper wiring. These results demonstrate the possibility of a common interconnect approach for advanced DRAM and logic and enable fabrication of future products such as merged logic - DRAM.

Design and Materials Directions

Hierarchical wiring architecture, featuring "fat" wires on the upper levels and thinner, tighter pitch wires at the lower levels, is expected to allow wire RC delay contributions to match future device performance increases, but will drive the addition of wiring levels faster than historical trends. Figure 2 shows an attempt to estimate the severity of this problem. An analysis of wiring length distribution and subsequent wireability was performed similar to that in reference 5. Two scaling cases are considered; first, the number of transistors in the system is constant, and second, the number of transistors increases by the scaling factor "s^2" per lithography generation to fill a chip of constant size. When similar calculations are done for Cu/low k interconnect systems, the number of wiring levels is greatly reduced (figure 2)

Many evaluations are currently underway in the area of low k dielectric integration. Most of the current work focuses on materials in the $2.5 < k < 3.8$ range, but as can be seen in figure 3, a continuous reduction in dielectric constant for IMD materials is required for future technology nodes. Each IMD material change will require a great deal of effort to execute, but without dielectric constant reduction, the impact on interconnect delay will be unacceptable in advanced devices (Fig. 4). In addition to the dielectric constant of the bulk IMD material, the dielectric constant of any additional barrier films or etch stops incorporated into the structure must also be reduced.

The use of the damascene method for patterning copper requires that a barrier/liner film acts as cladding on all but the top surface of the metallization. If the barrier thickness does not scale as the wiring scales, the impact on resistance will be significant. Figure 5 shows copper wiring resistance as a function of linewidth with various cladding film thickness. The resistance increase due to liner thickness becomes substantial for linewidths of approximately 0.2 υm and below. In order to address this problem, alternate methods of forming thin conformal liner films are needed such as CVD, electroless plating or alloying methods.

Summary

Materials, processing and architectural changes will be needed over the next few lithographic generations. Product commitments have been made to utilize copper interconnects and low k dielectrics and additional applications (e.g. DRAM) have been evaluated. Many additional process changes will be needed in order to enable performance enhancements in future generations.

Acknowledgment

The authors wish to thank our IBM colleagues for their hard work, dedication, innovation and for allowing us liberal use of their data.

References

1) L. Gwennap, Microprocessor Report, 8/4/97.
2) W. Cote et al. 1998 Symposium on VLSI Technology Digest of Technical Papers (The Japan Society of Applied Physics and The IEEE Electron Devices Society, Honolulu, pp. 24 - 25 (1998).
3) G. Bronner et al., 1995 Symposium on VLSI Technology Digest of Technical Papers (The Japan Society of Applied Physics and The IEEE Electron Devices Society, Kyoto, pp. 15 - 16 (1995).
4) C. W. Kaanta et al., IEDM Tech. Digest, pp. 209 - 212 (1987).
5) T. N. Theis, Presentation at 1998 Spring Electrochemical Society Meeting.
6) J. G. Ryan et al. Advanced Metallization and Interconnect Systems for ULSI Applications 1997 Conference Proceedings, R. Cheung, J. Klein, K. Tsubouchi, M. Murakami, and N. Kobayashi editors pp. 399 - 404, 1997.

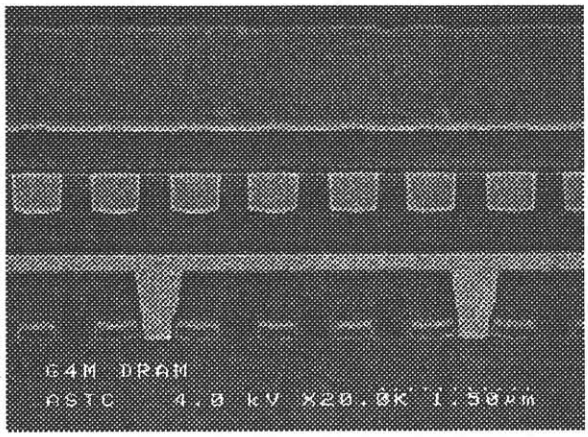

Fig 1. Cross sectional SEM of 64 Mb DRAM with M1 copper wiring.

Sample	Vt shift after anneal
17nm liner NFET device	-3 mV
17nm liner PFET device	+5 mV
30 nm liner NFET device	-2 mV
30nm liner PFET device	+3 mV
Al wiring NFET and PFET	ranges from +20mV to -20mV

Table I. Vt shifts of 4M DRAM with M1 copper wire after 400C anneal.

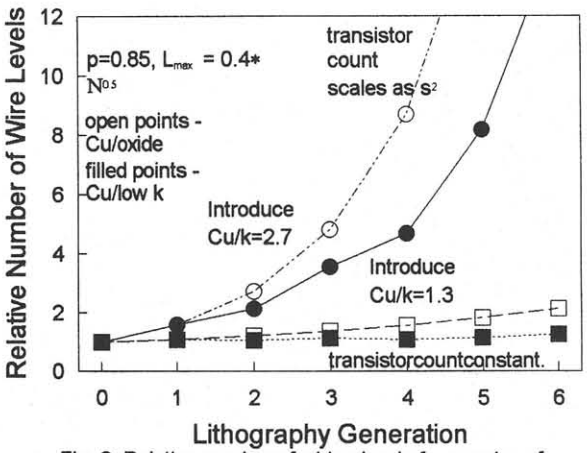

Fig. 2. Relative number of wiring levels for a series of wiring levels. (generation 0 is 0.50-0.35 υm)

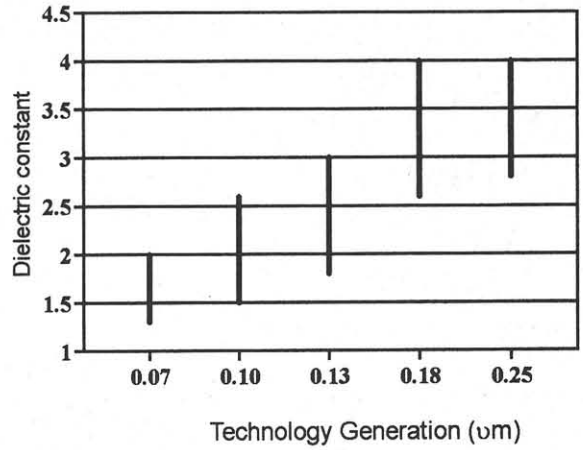

Fig. 3. Range of dielectric constant expected for current and future technology nodes.

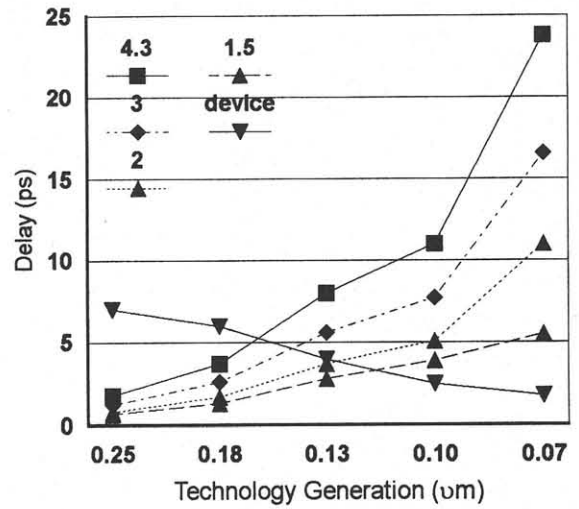

Fig 4. RC (ps per 0.1mm) at several effective dielectric constants. For comparison, gate delays are also shown.

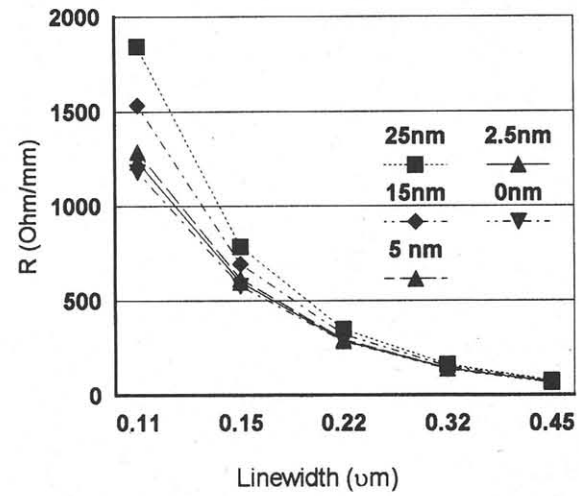

Fig. 5. Plot of resistance/mm of clad copper wires at different cladding thickness and linewidth