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Invited

Salicide Technologies for Deep-Sub-Micron-CMOS

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1. Introduction

Both Ti salicide and Co salicide processes are currently used by the ULSI industry in production of sub-0.25 μm CMOS. Ti salicide has been used for several generations, while Co salicide was introduced due to the increase in sheet resistance with decreasing linewidth observed for conventional Ti salicide. Pre-amorphization implants (PAI) [1, 2] and Mo doping [3-5] have been used to improve Ti salicide narrow line sheet resistance. While Co salicide does not have a linewidth effect [6, 7], it is more susceptible to diode leakage on shallow junctions [8] and GOI degradation, and is more sensitive to surface preparation. In this paper we present an overview of Ti and Co salicide processes developed to eliminate these scaling issues.

2. Ti Salicide

Conventional Ti salicide suffers from high sheet resistance at narrow linewdiths. This is due to incomplete transformation from high resistivity C49 $TiSi_2$ (~70 μΩ-cm) to the low resistivity C54 $TiSi_2$ phase (~15 μΩ-cm) on narrow lines [2]. The underlying cause is lack of C54 nucleation sites, mainly triple grain boundaries, on structures were the linewidth is smaller than the C49 grain size (~0.2 μm for conventional RTP) (Fig. 1) [2].

PAI induces a smaller C49 grain size (~0.07 μm), allowing easy transformation of 0.25 μm and enabling transformation of sub-0.25 μm lines (Fig. 2) [2]. However, the limit for application of PAI is ~0.1 μm gate length. In addition, drive current degradation is observed on devices with shallow junctions due to TED effects induced by PAI and thermal cycles with high thermal budget [4, 5].

An alternative method to improve narrow line sheet resistance is the use of Mo doping [3-5]. In this case the phase sequence is modified for poly-Si and amorphized-Si, so that C54 $TiSi_2$ grows directly bypassing the C49 phase Figs 3 and 4) [5]. In contrast, conventional C49 growth is seen on Mo doped (100) Si (Fig. 3) [5]. The mechanism of direct C54 growth was determined by HRTEM (Fig. 5): silicide phases ($MoSi_2$ and a phase likely based on Mo_5Si_3) nucleate at the Ti/Mo doped poly-Si interface, and grow to a layer thickness of ~5 nm. These phases then act as templates for epitaxial nucleation and diffusion limited growth of C54 $TiSi_2$ (Figs. 5 and 6).

Ti salicide with Mo doping alone has the drawback of bad thermal stability, with low agglomeration temperatures, and no direct C54 growth on S/D areas ((100) Si) [4, 5]. In contrast, the combination of Mo with low dose PAI, results in direct growth of C54 $TiSi_2$ both on gates and S/D (amorphized Si), and improves thermal stability compared to the Mo only case [5].

Fig. 7 shows sheet resistance vs gate length for various Ti salicide processes. The optimum process is a combination of low dose Mo and PAI and a low temperature one-step RTP, maintaining low sheet resistance to 0.06 μm gate lengths [5]. Direct C54 growth for Mo processes eliminates the issue of C49 to C54 transformation and its associated linewidth effect. For Mo without PAI, formation is difficult on sub-0.1 μm gates at low temperatures and agglomeration is an issue at higher temperatures, closing the process window [5].

3. Co Salicide

Co salicide does not suffer from a linewidth effect [6], maintaining low sheet resistance to 0.06 μm (Fig. 8) [7]. Surface preparation is a concern, and high resistance outliers can be found (independently of gate length) if surface preparation is not optimized. High diode leakage on shallow n+/p junctions is the main scaling problem for Co salicide, due to non-uniform silicidation reactions that can lead to spiking [8] and rough interfaces [7]. A more uniform silicidation is obtained with optimized high temperature RTP, eliminating the diode leakage problem (Fig. 9) [4, 7, 8]. In addition, Co is also more susceptible than Ti to GOI issues. Non optimal Co processes can result in severe GOI degradation, not observed in general for a wide range of Ti processes. However, process optimization (mainly thermal history), eliminates this problem (Fig. 10).

4. CMOS Device Performance

Fig. 11 shows the implementation of optimized Co and Ti salicides into a 0.12 μm, 1.5 V CMOS technology achieving high drive currents (~720 and 315 μA/μm at I_{OFF}=1nA/μm, for nMOS and pMOS respectively) [5].

5. Conclusions

Optimization of advanced salicide processes, makes both Ti and Co salicides compatible with deep-submicron technologies, achieving low sheet resistance on 0.06 μm gates, with low diode leakage and high drive currents.

References

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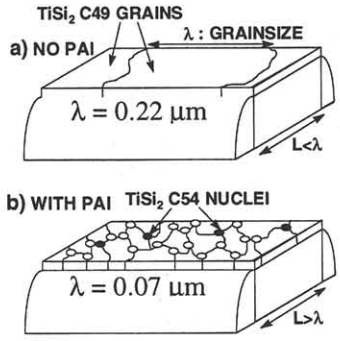


Fig. 1. Pre-amorphization implants (PAI) induce a smaller C49 $TiSi_2$ grain size. Nucleation of low resistivity C54 $TiSi_2$ at triple grain boundaries is then possible for sub-0.25 μm gate lengths.

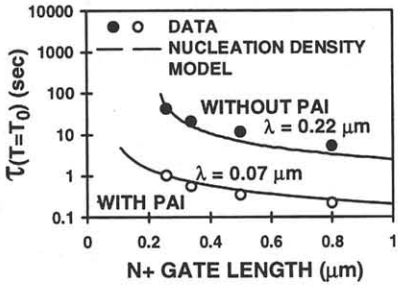


Fig. 2. Half-transformation times for the $TiSi_2$ C49 to C54 transformation. A decrease in transformation times with PAI of ~two orders of magnitude on deep submicron gates is explained by a nucleation density model, based on the average number of triple grain boundaries.

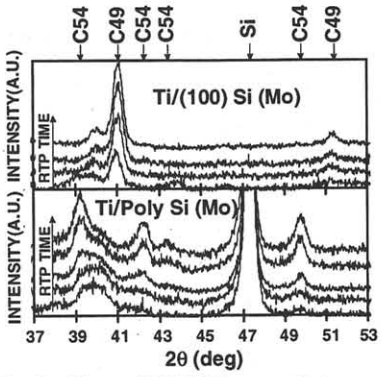


Fig. 3. Direct C54 $TiSi_2$ growth bypassing C49 $TiSi_2$ is seen on Mo doped poly-Si at 650°C. In contrast, conventional C49 $TiSi_2$ growth is seen on Mo doped (100) Si.

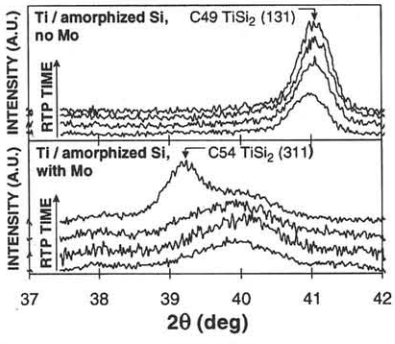
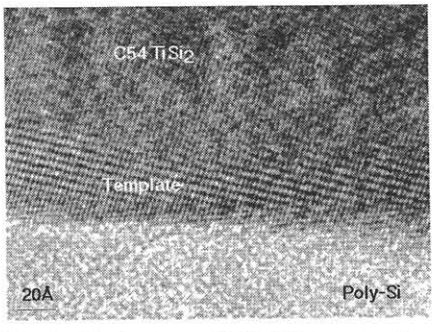


Fig. 4. Direct C54 growth bypassing C49 $TiSi_2$ on Mo doped amorphized Si. C49 grows on amorphized Si without Mo .



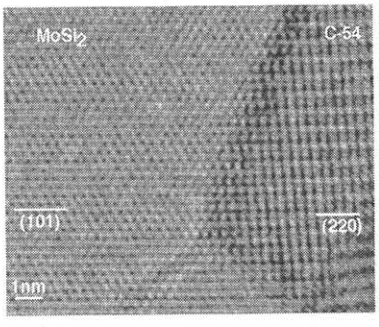


Fig. 5. Mechanism of C54 $TiSi_2$ nucleation bypassing C49 $TiSi_2$ on Mo doped poly-Si: Mo silicide phases (left: phase based on Mo_5Si_3, right: $MoSi_2$) nucleate at the Ti-Si interface and act as templates for epitaxial C54 $TiSi_2$ growth.

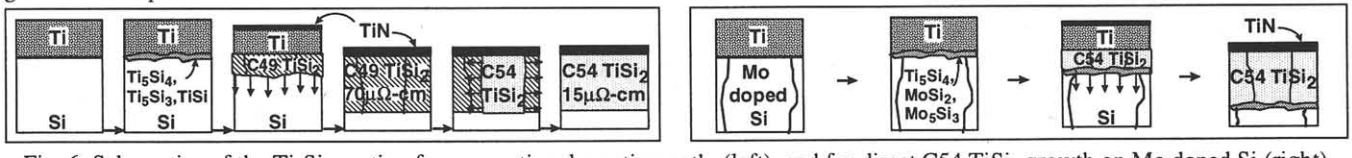


Fig. 6. Schematics of the Ti-Si reaction for conventional reaction path (left), and for direct C54 $TiSi_2$ growth on Mo doped Si (right).

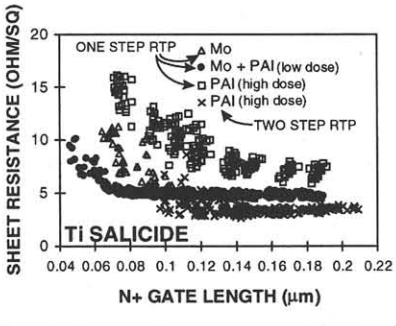


Fig. 7. Sheet resistance vs gate length for Ti salicide. One-step RTP with Mo and PAI maintains low resistance to 0.06 μm.

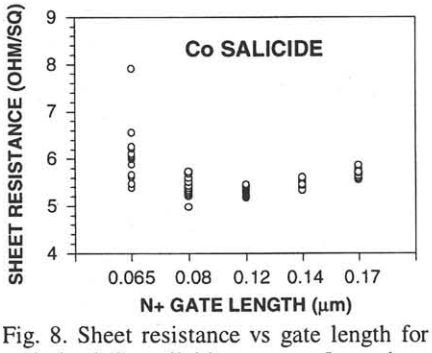


Fig. 8. Sheet resistance vs gate length for optimized Co salicide process. Low sheet resistance is maintained to 0.06 μm.

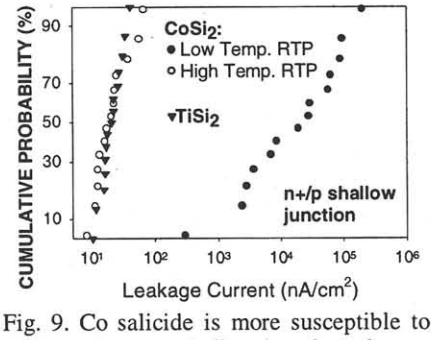


Fig. 9. Co salicide is more susceptible to diode leakage on shallow junctions, but an optimized RTP eliminates high leakage.

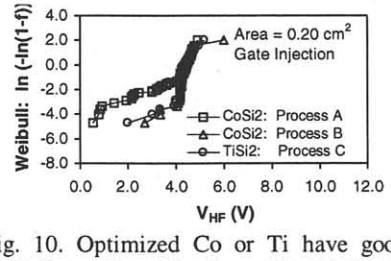


Fig. 10. Optimized Co or Ti have good GOI. Non-optimal Co shows degradation.

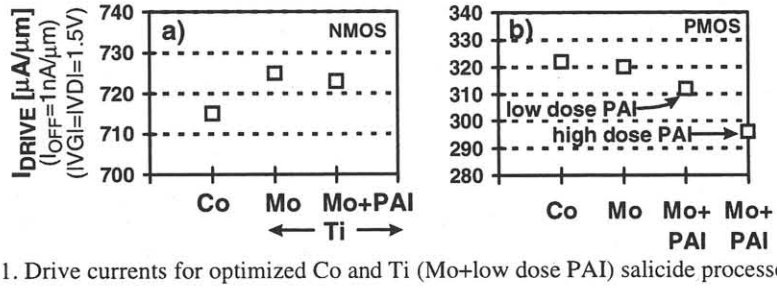


Fig. 11. Drive currents for optimized Co and Ti (Mo+low dose PAI) salicide processes.