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Low Contact Resistance Poly-Metal Gate CMOS Using TiN/Thin $TiSi_2$/Poly-Si Structure

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1. Introduction

For deep submicrometer MOSFETs with low gate sheet resistance and high heat resistance, poly-metal gate electrode structures, such as W/WN/poly-Si[1] ,W/TiN/poly-Si[2] and TiN/poly-Si[3] have been demonstrated. Contact resistance between metal and poly-Si is a key issue in these poly-metal gate structures. It is known that gaining the ohmic contact between TiN and silicon is especially difficult[4]. This high contact resistance causes a degradation of the MOSFETs' performance[5]. From simulations of CMOS ring oscillators, a contact resistance of less than 300 $\Omega\mu m^2$ is necessary to suppress a delay time degradation of less than 10 % as shown in Fig.1.

In this paper, we propose a low contact resistance poly-metal gate structure by inserting a thin $TiSi_2$ layer between TiN and poly-Si. In order to confirm this structure's feasibility, nMOSFETs and pMOSFETs with this type of gate electrode were fabricated.

2. Experimental Results

The structure of this new gate electrode is shown in Fig .2. After gate doping by ion implantation and activation annealing, thin Ti was sputtered for improving the contact resistance between TiN and poly-Si. $TiSi_2$ was formed during gate cap LTO and RTA process.

To investigate a suitable thickness for inserted Ti, the contact resistance between TiN/$TiSi_2$ and n^+poly-Si was measured with a parameter of Ti sputtered thickness. This result is shown in Fig.3. The thinner the Ti sputtered thickness is, the lower is the contact resistance. For a Ti thickness of 5 nm, a contact resistance as low as 130 $\Omega\mu m^2$ was obtained. In order to find the reason for this result, SIMS measurements were made. The results are shown in Fig.4. The thicker $TiSi_2$ layer absorbs a higher amount of phosphorus that was implanted in poly-Si, and the decreased phosphorus concentration of the interface induced a high contact resistance.

Then, nMOSFETs and pMOSFETs with this gate structure were fabricated with 65 nm TiN layer. The process flow is shown in Table 1. For 65 nm TiN thickness, the sheet resistance was 10Ω/sq. and stayed constant for gate lengths down to 0.1 μm as shown in Fig.5. As shown in Fig.3 the sputtered Ti thickness in this fabrication process was 5 nm. BCl_3 and Cl_2 for the TiN/$TiSi_2$ layer, and HBr and O_2 for poly-Si were the gate etching chemis try,respectively. Fig.6 shows a SEM photomicrograph of the final MOSFET cross section. A 0.08μm long gate was successfully etched on 4 nm gate oxide.

Fig.7(a) shows the short channel effect of nMOSFETs and pMOSFETs. Fig7(b) shows Id-Vg characteristics. These characteristics were almost the same as for the conventional poly-Si gate structure. In order to evaluate lateral dopant diffusion through the $TiSi_2$ layer, we measured Vth shift as a function of the distance from the opposite impurity source. The results are shown in Fig.8(a),(b). The dopant lateral diffusion of this gate structure was comparable with a conventional poly-Si gate for both nMOSFETs and pMOSFETs. This is because $TiSi_2$ thickness is thin enough to prevent the dopant from moving through the $TiSi_2$ layer.

3. Conclusion

A new gate electrode structure of TiN/$TiSi_2$/poly-Si was proposed. By using 5 nm Ti in order to form a thin $TiSi_2$ layer, the contact resistance between TiN and poly-Si can be sufficiently lowered to be accepted. nMOSFETs and pMOSFETs with the proposed gate structure that have a 4 nm gate oxide were fabricated. We showed that these MOSFETs have the same characteristics as a conventional poly-Si gate.

Acknowledgments

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References

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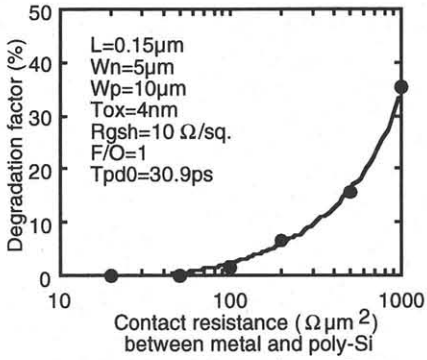

Fig.1 Tpd degradation on ring oscillator by metal/poly Si contact resistance

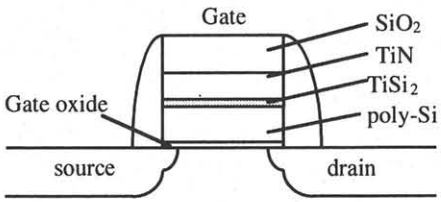

Fig.2 Structure in this study

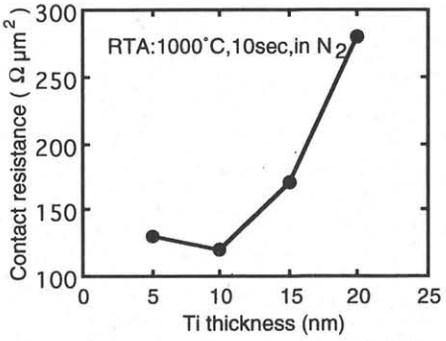

Fig.3 Contact resistance between TiN/TiSi $_2$ and poly Si versus Ti sputtered thickness

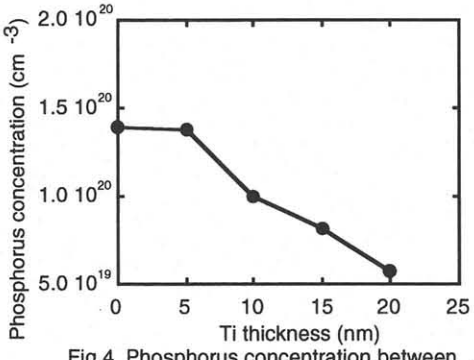

Fig.4 Phosphorus concentration between TiSi$_2$ and n+poly Si versus Ti Sputtered Thickness

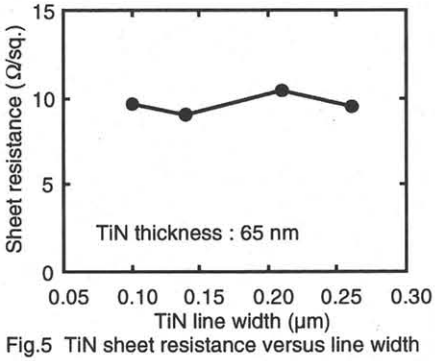

Fig.5 TiN sheet resistance versus line width

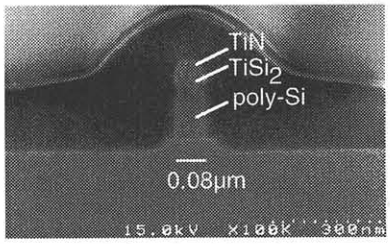

Fig.6 SEM photomicrograph of the final MOSFET cross section
Gate length : 0.08μm

Table 1 Process flow of TiN/TiSi$_2$ /poly Si gate MOSFET

- Isolation
- Well and Channel Formation
- Gate Oxidation : 4nm
- Poly Si Deposition : 180nm
- Gate Ion Implantation
- Activation Annealing
- Ti sputtering : 5nm
- TiN sputtering : 65nm
- LTO Deposition
- Gate RIE
- LDD Ion Implantation
- LTO Sidewall formation
- S/D Ion Implantation
- LTO Deposition
- RTA : 1000°C,10sec, in N_2
- Metallization

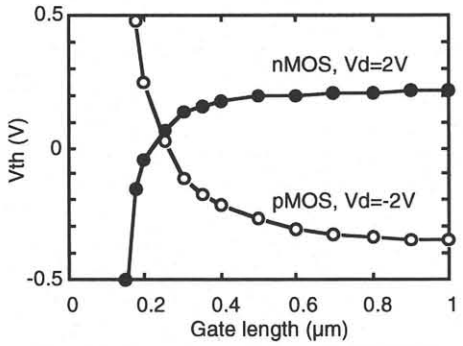

Fig.7(a) Short channel effect of nMOSFETs and pMOSFETs

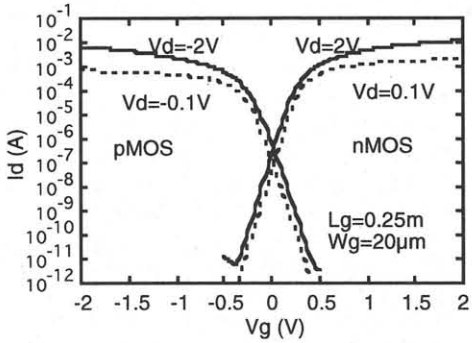

Fig.7(b) Id-Vg characteristics of nMOSFET and pMOSFET

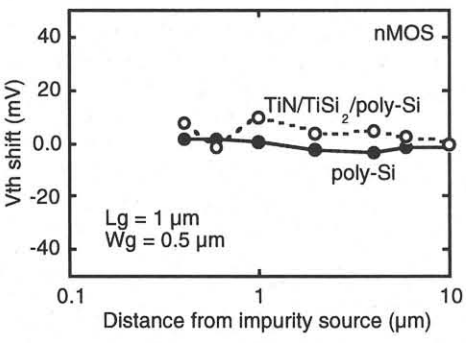

Fig.8(a) Vth shift of nMOSFETs as a function of distance from opposite impurity source

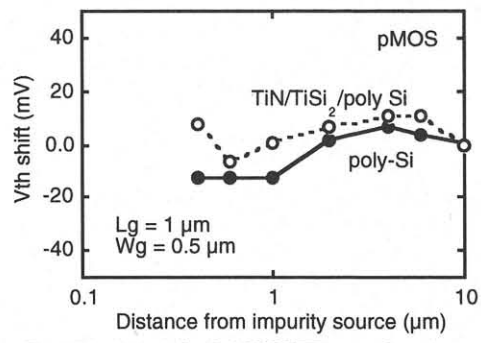

Fig.8(b) Vth shift of pMOSFETs as a function of distance from opposite impurity source