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A Novel Clean Ti Salicide Process Using Grooved Gate Structure

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1. Abstract

This paper demonstrates that dry etching or Ar sputtering causes phase transition failures of $TiSi_2$ and degradation of the sheet resistance. It is because contaminations are introduced on gate surface by these treatments. We propose a Ti Salicide on grooved gate process. In this technique poly-Si is patterned by a PSG mask and the poly-Si surface is not exposed by Ar sputtering before Ti deposition. The PSG layer protects gate surface from the contaminations by dry etching for sidewall formation. As a result, agglomeration of $TiSi_2$ was suppressed and low sheet resistance of 14 ohm/sq. was obtained at a 0.12 μm line width.

2. Introduction

Ti Salicide(Self-aligned-silicide) process has been widely used to improve the performance of CMOS logic devices. However, it is well known that the sheet resistance(Rs) of $TiSi_2$ increases at a narrow gate by phase transition failures and agglomeration. Contaminations such as fluorine, carbon and oxygen will be introduced on Si surface by various treatments during fabrication, and these contaminations are supposed to affect the increase of $TiSi_2$ resistance[1,2]. Using oxygen and fluorine free process(DTD process), the Rs of a 0.1 μm gate became quite low[3]. However, this process is very complicated and would not be practical.

In this paper, we propose a Ti Salicide on grooved gate[4] process to reduce the contaminations(Figure 1)[5]. The key issue of this technique is the protection of gate surface from contaminations instead of removing a contaminated layer. To fabricate grooved gate structure, poly-Si is patterned by a PSG mask. After sidewall (NSG) formation by dry etching, the PSG mask, which protects poly-Si surface from contaminations by the dry etching, is selectively etched by DHF. Before Ti deposition, poly-Si surface is only treated with DHF and is not exposed to Ar sputtering. $TiSi_2$ is formed by PAI(Pre-amorphization implantation) and 2step annealing[6]. By using this technique, we can also investigate the influence of contaminations only by Ar sputtering on Rs of $TiSi_2$.

At first, contaminations on Si surface introduced by dry etching or Ar sputtering were evaluated. Secondly, resistivity and crystal structure of $TiSi_2$ on Si were investigated. At last, the influence of dry etching and Ar sputtering on Rs of $TiSi_2$ at a narrow gate was investigated.

3. Experiments and discussion

3-1. Contaminations and $TiSi_2$ on Si

Three types of samples (Sample A,B,C) were prepared for analysis of contaminations and $TiSi_2$ on Si. In Sample A, 200 nm thick PSG was deposited on Si. After 250 nm thick NSG was deposited on a PSG layer, NSG was removed by dry etching using CHF_3 and CF_4 gases. The remained PSG layer was etched by DHF. This process is equivalent to fabricate grooved gate structure. In Sample B, Ar sputtering was added after the same process of Sample A. Si surface was only damaged by Ar sputtering. In Sample C, a PSG layer was not deposited on Si. Si surface was damaged by dry etching. After these treatment Ti/TiN(100 nm/30 nm) was deposited, and annealed at 700 °C in a N_2 atmosphere for 5 or 30 sec. Contaminations on Si surface were analyzed by XPS. Resistivity of $TiSi_2$ was measured from the thickness of film and the resistance. Crystal structure of $TiSi_2$ was measured by XRD. Figure 2 shows the result of XPS analysis. The intensity of fluorine, carbon and oxygen were all lower in Sample A than Sample B and C. Figure 3 shows resistivity of $TiSi_2$ on the samples. After 5 sec. of annealing, the resistivity was not so different from one another, but after 30 sec. only the resistivity of Sample A became much lower. It suggests that C49 transformed to C54 only in Sample A. Figure 4 shows XRD patterns of $TiSi_2$ on the samples. $TiSi_2$ was actually transformed from C49 to C54 only in Sample A. It is supposed that oxygen prevents the phase transition, because the intensity of fluorine and carbon were not so different between Sample A and B(Fig.2).

From these results, it was clarified that dry etching and even Ar sputtering caused contaminations and suppressed phase transition of $TiSi_2$, although Ar sputtering was used for Si surface cleaning. With a Ti Salicide on grooved gate process, these contaminations will be reduced and the Rs of $TiSi_2$ at a narrow gate line will decrease.

3-2. $TiSi_2$ on poly-Si gates

The dependence of Rs on gate line width was investigated. Three types of samples were prepared by similar processes mentioned in section 3-1. As implantation was carried out at 100 keV and 5e15 cm^{-2} without oxide cap layer after a PSG mask was removed.

It was clarified that dry etching or Ar sputtering suppressed phase transition of $TiSi_2$ and accelerated agglomeration on a narrow gate as shown in Figure 5. These treatments are supposed to introduce contaminations on poly-Si surface. By using a Ti Salicide on grooved gate process, agglomeration of $TiSi_2$ did not occur at a narrow gate, and low Rs of 14 ohm/sq. was achieved at a 0.12 μm line width.

4. Summary

It was clarified that Si surface is contaminated by dry etching or Ar sputtering. To protect gate surface from contaminations, we proposed a Ti Salicide on grooved gate process. With this technique, the contaminations on gate surface were reduced and the anomalous increase in Rs of $TiSi_2$ at a narrow gate could be suppressed.

References

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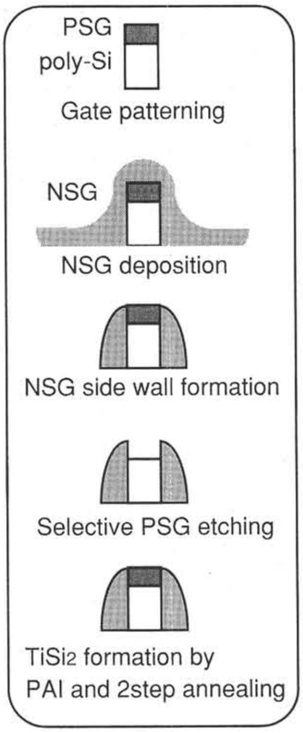

Fig. 1 Schematic process flow for grooved gate structure and $TiSi_2$ film formation

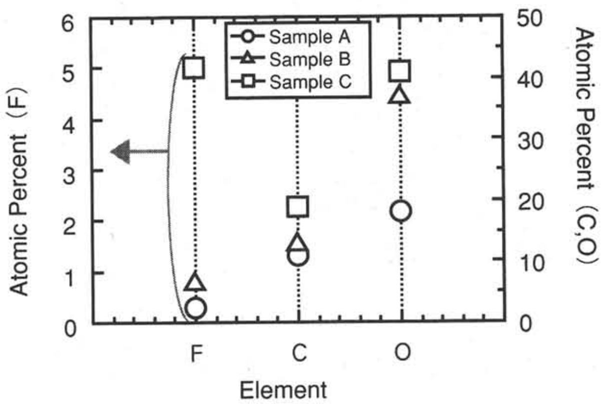

Fig. 2 : XPS intensity of fluorine, carbon, and oxygen on the Si surface

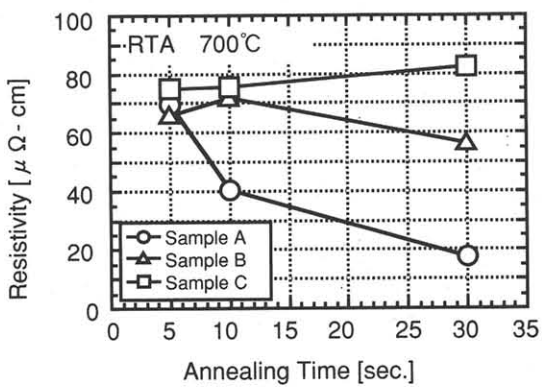

Fig.3 Annealing time dependance of $TiSi_2$ resistivity

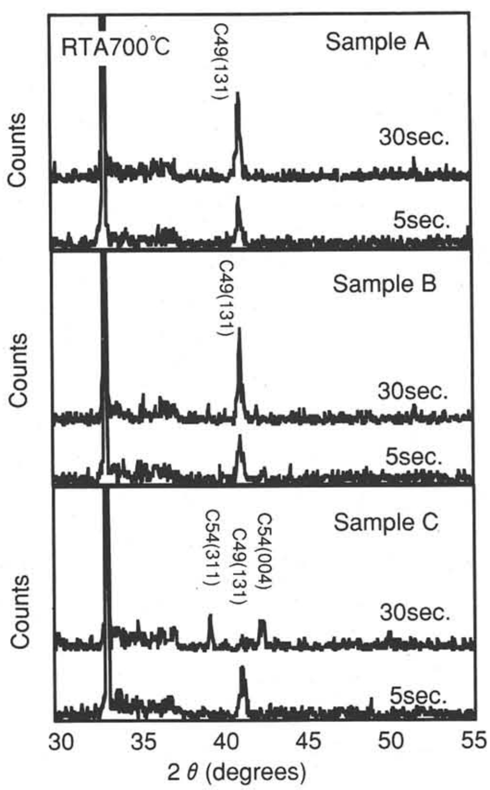

Fig. 4 : XRD patterns of $TiSi_2$ formed by annealing at 700℃ for 5 or 30 sec.

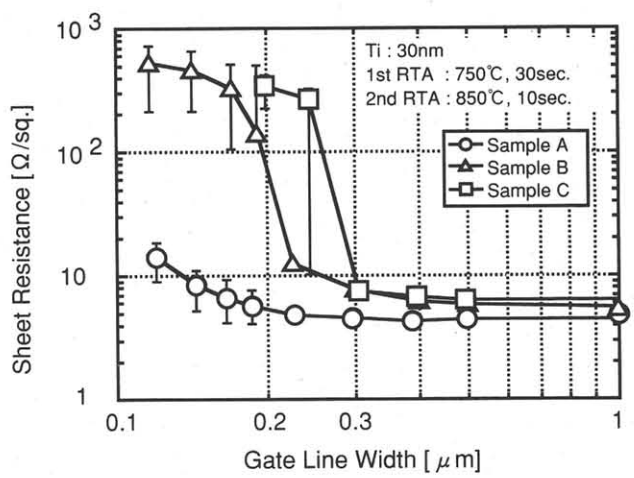

Fig. 5 : Sheet resistance of $TiSi_2$ on n^+ gates as a function of the gate line width