Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 278-279 **A-7-5**

Highly Uniform Deposition of LP-CVD 3i3N4 Films on Tungsten for Advanced Low Resistivity "Poly-Metal" Gate Interconnects

Yasushi Akasaka, Kiyotaka Miyano, Kazuaki Nakajima and Kyoichi Suguro
Microelectronics Engineering Laboratory, Toshiba Corp., 8, Shinsugita-cho, Isogo-ku, Yokohama 235, Japan
Phone: +81-45-770-3663, Fax: +81-45-770-3577, E-mail: yasushi.akasaka@toshiba.co.jp

1. Introduction

In advanced ULSI's, low resistivity gate interconnects are strongly required to suppress gate RC delays. Currently, SALICIDE (self aligned silicide) and polycide gate structures are widely used to achieve a sheet resistivity of 5-10 Ω/□ . To realize lower sheet resistivity of 1-2 Ω/□ or comparable sheet resistivity with lower gate height, a new gate structure is necessary.

We propose a poly-Si/ WSiN barrier layer/ W multilayered gate structure (poly-metal). [1] [2] We can achieve a low resistivity of 1.4 Ω/□ with a poly-metal structure (poly-Si(700nm) / WSiN (50nm) / W (100nm)) and comparable resistivity of 5 Ω/□ with an extremely thin poly-metal structure (poly-Si(700nm)/ WSiN (50nm)/ W (450nm)).

Moreover, to obtain reduced chip size, SAC (self aligned contact) structure is applicable to poly-metal gate as adopting Si_3N_4 cap and spacers. Thus a poly-metal structure with Si_3N_4 cap and spacers is extremely suitable for 1G-DRAM or later generation LSIs. (Fig. 1)

For the purpose of forming the cap and spacers, an LP-CVD Si_3N_4 film has several merits, e. g. good coverage, low impurities and high thermal stability. However, an abnormal growth of Si_3N_4 film on W easily occurs. (Fig. 2) We found out the abnormal growth is caused by the oxidation of W surface.

In this paper, we will show the process of the abnormal growth and propose methods for highly uniform deposition of Si_3N_4 films.

2. Abnormal growth of an Si_3N_4 film on W

Si_3N_4 deposition is carried out with vertical-type LP-CVD furnace. The sequence of deposition is shown in Fig. 3. Si wafers should be loaded below 550°C. At temperatures higher than 550°C ,W is easily oxidized and the expansion when W oxide is formed causes film peeling.

The process of abnormal growth is investigated. Fig. 4(a) and (b) show W surface before and after Si_3N_4 deposition. During heating up in N_2 ambient up to the deposition temperature (780°C), whiskers are formed on W surface and Si_3N_4 is conformally deposited on whiskers. Thus granular surface of Si_3N_4 film is formed. As described below, this effect is strongly dependent of the amount of oxygen at the interface of W and Si_3N_4. Hence these whiskers are considered to be W oxide.

3. Suppression of abnormal growth

There should be two ways to suppress abnormal growth of Si_3N_4 films; 1) suppression of W surface oxidation before deposition 2) in-situ reduction of W oxide before deposition.

Oxidation suppression method (Low temperature load-in)

In order to prevent oxidation of W surface, low temperature load-in is tried out. The morphology of Si_3N_4 surface is much improved by lowering load-in temperature down to 350°C.(Fig. 5(a)-(c))

In-situ reduction of W oxide

In-situ reduction method in NH_3 ambient is examined. In order to clarify its effect , load-in temperature is raised to 400°C. NH_3 flow is provided at a temperature that the morphological change of W surface would not be so severe (600°C). Fig. 6(a)-(c) shows surface of Si_3N_4 on some NH_3 reduction conditions. It is clearly shown that the NH_3 reduction improves Si_3N_4 morphology. Fig 7(a)-(c) show SIMS profiles of Si_3N_4/W interface. By 30Torr, 30 min. NH_3 flow, the amount of oxygen at the Si_3N_4/W interface could be decreased to about the same amount of 350°C loaded wafer which has smooth Si_3N_4 surface as shown in fig. 5(c).

4. Discussion

It is shown that the two methods mentioned above are both useful to suppress abnormal deposition of Si_3N_4 film on W. It is considered to be essential that the amount of oxygen at the Si_3N_4/W interface be decreased. Load lock chamber and inert gas purge chamber are also thought to be effective to prevent oxidation of W surface. However, we think the method of in-situ reduction is superior to the methods of preventing oxidation of W surface. Because it is thought to be difficult to control the surface condition of W with oxidation suppression methods just before deposition starts. If an oxidation suppression method can be used, it is desirable to use in-situ reduction method together with it.

5. Conclusion

For the formation of poly-metal gates with Si_3N_4 cap/spacers, a uniform deposition technique of LP-CVD Si_3N_4 on W is necessary. An abnormal growth of Si_3N_4 occurs when W surface is oxidized. Two methods are demonstrated for suppressing abnormal growth. Both oxidation suppression method and in-situ reduction method are effective. However, in-situ reduction method is considered to be suitable to control surface oxidation of W just before Si_3N_4 depositions.

By using the in-situ reduction method, poly-metal structure with Si_3N_4 cap/spacers can be successfully formed. And this structure should be extremely useful for the ULSIs of 1G-DRAM and later generation.

Acknowledgments

The authors would like to thank Y. Kasai, J. Shiozawa , T. Kai, Y. Tsunashima and M. Kiyotoshi for continuous discussion and M. Takahashi, T. Hatanaka and S. Tanaka for technical assistance. And we also acknowledge A. Azuma, Y. Hiura, M. Takagi, K. Agawa, K. Kasai, H. Oyamatsu, N. Yoshimura, H. Koike, M. Kinugawa, Dr. F. Matsuoka, Dr. K. Okumura and Dr. T. Arikado for helpful discussion and continuous encouragement.

Reference

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2) K. Nakajima, Y. Akasaka, K. Miyano, M. Takahashi, S. Suehiro and K. Suguro: Appl. Surf. Sci. **117/118** (1997) p. 312

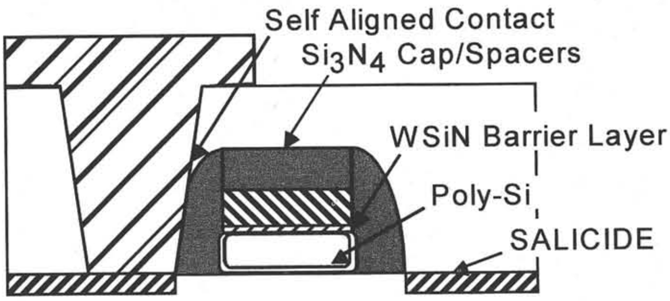

Fig. 1 Concept of self-aligned contact technique of poly-metal with Si_3N_4 cap/spacers.

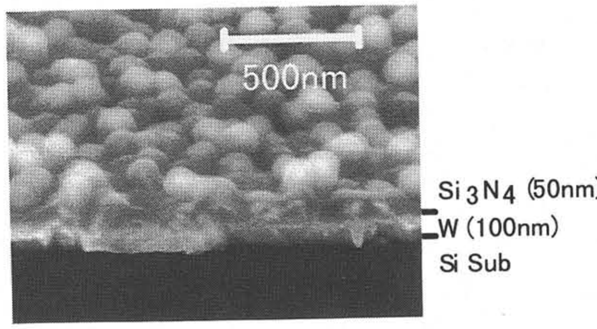

Fig. 2 Abnormal growth of LP-CVD Si_3N_4 on W.

- Wafer load in (< 550°C)
- Evaculation (< 1m Torr)
- Heat up (780°C)
- Heat recovery (~30 min.)
- Deposition
(780°C, NH_3/SiH_2Cl_2 = 10/1, 0.5 Torr)
- Evaculation (< 1m Torr)
- Cool down

Fig. 3 A typical sequence of LP-CVD Si_3N_4 deposition on W.

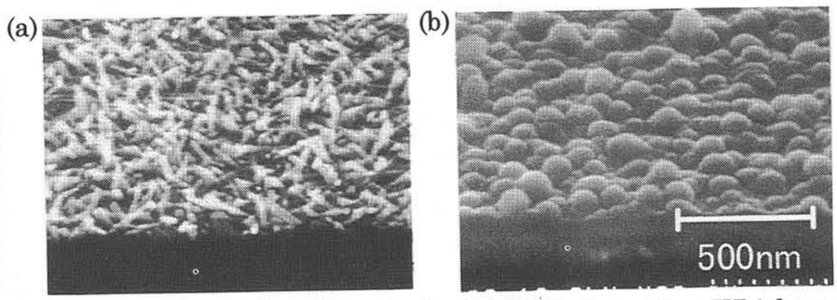

Fig. 4 W surface before (a) and after (b) Si_3N_4 deposition. Whiskers are observed on W surface before deposition.

Fig. 5 Surface morphology of low-temperature load-in Si_3N_4 films on W. (a) 450°C (b) 400°C (c) 350°C

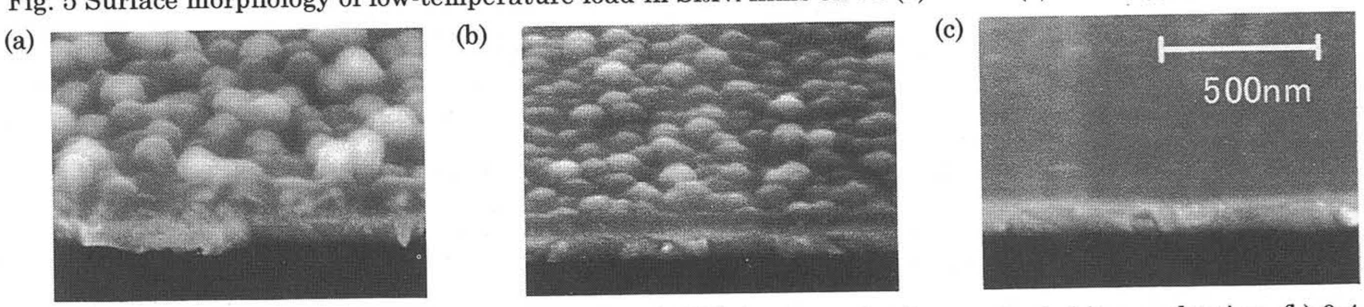

Fig. 6 Surface morphology of Si_3N_4 surface on W with NH_3 in-situ reduction method. (a) no reduction (b) 0.4 Torr 30 min. reduction (c) 30Torr 30min. reduction.

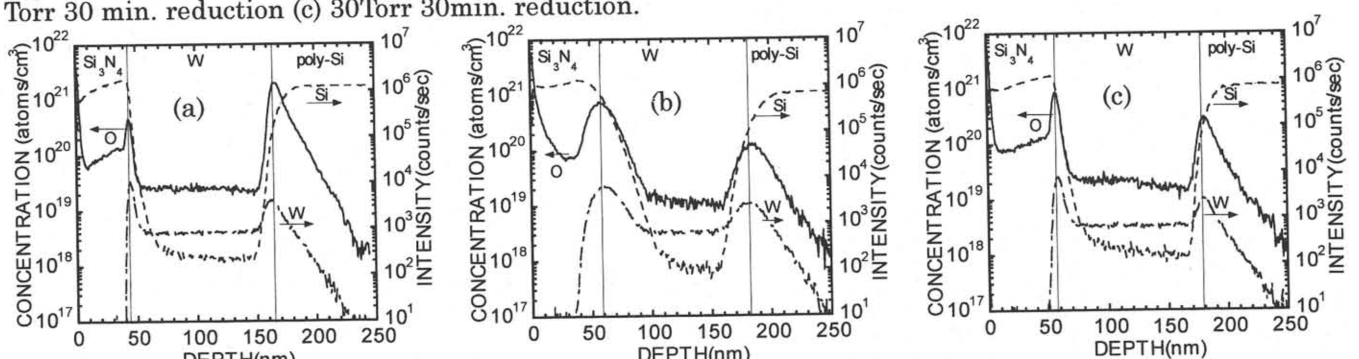

Fig. 7 SIMS profiles of Si_3N_4 on W with NH_3 in-situ reduction method (a) 0.4Torr 30 min. reduction (b) 30Trorr 30 min. reduction (c) ref. 350C load-in, no NH_3 reduction.