Multilevel Aluminum Dual-Damascene Interconnects (Al-DDI) for Process-Step Reduction in 0.18μm-ULSI

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1. Introduction

The total number of interconnect layer has increased with integrating ULSIs, resulting in abrupt increment of the ULSI fabrication process step. In addition, especially for 0.18 μm generation, KrF (248nm) stepper and photo-sensitive resist are used in photo-lithography, and the reflection from the lower layer patterns has to be seriously cared. Usually, organic anti-reflection coating (ARC) film is used, but the dry-etching is very difficult by the photo-resist mask.

Main purpose of this paper is process-step reduction for the multilevel interconnects with wide tolerance of via-contacts. Here, a new process is proposed for dual-damascene interconnects (DDI), in which the interlayer dielectric (ILD) film structure is simplified to eliminate the organic ARC film in the photo-lithography.

2. Process Design of Multilevel Interconnects

Figure 1 shows schematic illustration of conventional interconnects (type I) and DDIs (type II, and III). In type I, misalignment between Via1(W) and M2(AI) during the lithography causes connection area small in borderless-via structure, increasing the via-resistance. Organic ARC-film, however, is not necessary because TiN film on Al-interconnects underlaid prevents reflection during KrF lithography. DDI-strutures, on the other hand, are supposed to reduce the process-step because the hole-via and the line-trunch are simultaneously filled with metal. In the ordinal DDI (type II), the complicated ILD-film structure of SiO2/SiN(a stopper for line-trench etching)Si3N4 is needed, thus increasing the process step. Furthermore, organic ARC-process is necessary to prevent reflection from the CMP-derived flat metal-layers without surface-TIN. The process step in type II is as large as that in type I as shown in Fig. 2.

In type III, the ILD-structure is simplified as the lamination of SiO2/SiON, in which the SiON for the via areas is utilized not only as the stopper of line-trench etch, but also as an absorbent for the reflection during KrF-lithography. Figure 3 shows the via-hole diameter of photo-resist as a function of the relative SiON thickness in the via area. The total film thickness of via area was fixed as 300nm-thick. The hole-diameter on the ILD without any SiON film was 1.5 times as large as the designed mask-diameter of 0.28 μm by under an overdose exposure condition, and decreased with increasing SiON film until 200nm-thick. This means that the SiON film over 200nm-thick suppresses the reflection-light from Al-film.

Type III structure was fabricated by the via-hole etch followed by the line-trench etch. Subsequently, Al-filling was performed by hot aluminum sputter [1]. Finally, Al-DDIs were fabricated by Al-CMP. 17% reduction in the process step was accomplished for the type-III DDIs with 300nm-thick SiON in the via area due to no need for the organic ARC process. Figure 4 shows cross sectional BSEM (back scattering electron microscope) image of 4-level Al-DDIs in SiO2/SiON ILD-film (type III). The minimum line-pitch was 0.56 μm for M2—M4. The M1 was designed to be thickened for the single-damascene interconnects (SDI).

3. Characteristics of the Al-DDI

Figure 5 shows the line width dependence of line resistance in M1-SDI and M4-DDI. The M4-DDI with the minimum line-width of 0.24 μm was confirmed. The line resistance of M4 (360nm-thick), however, was about 2.2 times larger than that of M1 (470nm-thick) due to not only their thickness difference but also the formation of thicker Al/Ti alloy [2]. This is because thick Ti-liner (30nm) was needed for the deeper Al-filling in M4-DDI than that in M1-SDI.

Figure 6 shows the via size dependence of the via resistance. The via resistance at 0.28μm6 was 1—2Ω/via, which was much lower than that of tungsten via in type I [3]. Furthermore, the type III Al-DDI had smaller via-resistance of borderless-via structure than that of the conventional pad-via structure as shown in Figs. 7 and 8. In the pad-via structure, the vias are always connected to the lower Al-DDI surface, which is supposed to have CMP damage. In the borderless-via, the via is connected not only to the Al-DDI surface but also to the side-wall. Increment of the effective connection area is one of the reasons for the low resistance. The borderless structure was still effective in the three-layer stacked borderless-vias from M2 to M4 as shown in Fig. 9.

4. Conclusions

Four-layered Al-DDI is fabricated with a simplified ILD structure of SiO2/SiON lamination to reduce the process step; the SiON film acts as not only the stopper for line trench etch in the SiO2, but also the absorbent for the reflection during KrF-lithography, thus eliminating the organic ARC process. The 17%-reduction in the fabrication process step is accomplished. The multilevel Al-DDI has small via-resistance for the borderless structure of 0.28 μm6 by the line-side-wall contacts. The borderless structure is also effective in the stacked-vias chains penetrating from three interconnect layers from M2 to M4. The Al-DDI process pushes the fabrication cost-down, especially, for low-end logic ULSI in 0.18 μm-era.

References

3) A. J. McGeown, Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, 635.
Type I

Type II

Type III

Conventional

Dual Damascene

Fig. 1 Schematic illustration of the conventional (type I) and the dual damascene (type II, III) interconnects. Type III with the simplified ILD structure of SiO₂/SiON lamination is proposed in this study for process-step reduction.

Fig. 2 Comparison of number of process-steps among type I, II and III as shown in Fig. 1.

Fig. 3 SiON thickness dependence of the measured resist hole-diameter after KrF(248 nm) lithography.

Fig. 4 Cross sectional BSEM image of four level aluminum dual-damascene interconnects (type III).

Fig. 5 Line-width dependence of the resistance in M1 and M4 in the type III Al-DDI.

Fig. 6 Resistances of Al-via in the type III Al-DDI and W-via in the conventional interconnect (type I) [3].

Fig. 7 Schematic illustration of the "pad via" and the "borderless via" in type III DDIs.

Fig. 8 Resistance of the "pad via" and the "borderless via" in the type III Al-DDI as shown in Fig. 7.

Fig. 9 Dot size dependence of chain resistance for the stacked vias through the 3-interconnect layers. The "dot" is the dot line in M3. The "D=0" reveals the stacked-borderless-via of Via2 and Via3.