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Ultra-Low Ressitance, Through-Wafer Via (TWV) Technology and Its Applications in Three Dimensional Structures on Silicon

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Abstract

This paper presents an ultra-low resistance, high wiring density, through-wafer via (TWV) that is compatible with standard semiconductor processing. The via is 30 μm in size, and the resistance is less than 50 mΩ/via through a 525-μm thick wafer. Fabrication steps include through-wafer dry etching of high aspect ratio vias, copper metallization, and photoresist electroplating. Novel, three dimensional (3D) inductors are fabricated using this technology to demonstrate high quality factor (Q).

1. Introduction

There is a broad range of potential applications for low resistance through-wafer vias (TWV's) [1] such as interconnects in circuits, 3D packaging (e.g., stacking), and fabrication of 3D electrical and MEMS structures. Through-wafer vias should be evaluated with respect to size, resistance, and compatibility with standard semiconductor processing. To address the above issues, we have developed a fabrication process, which involves etching, conformal metallization, and patterning of high-aspect ratio TWV's. We demonstrate its features by fabricating a set of novel, integrated, 3D inductors and report on their characteristics.

2. Process Integration

The TWV process is outlined in Fig. 1. The substrate is a p-type, 4-inch, 525-μm thick, 10-Ω-cm, double-polished silicon wafer. We etch a 30-μm wide square TWV (Fig. 1a) which has an aspect ratio of greater than 17:1. The via size is similar to that of a contact pad. The reactive ion etching (RIE) is performed using a silicon deep trench etcher (STS Limited, UK) with 16-μm thick photoresist as the mask. The etch rate is 2.2 μm/min. To isolate each via electrically, 1-μm thick thermal oxide is grown. Then, 1.5-μm thick undoped polysilicon is deposited using low pressure chemical vapor deposition (CVD) (Fig. 1b). The polysilicon serves as the seed layer for the 250-nm thick CVD copper. Next, 6-μm thick copper is electroplated conformally on the CVD copper (Fig. 1c). The resulting sheet resistance is 2.8 mΩ/□. For patterning both sides of the wafer, while protecting the inside of the metallized vias, we use a 7-μm thick electro-plated photoresist (PEPR 2400, Shipley Co, MA) (Fig. 1d). A conventional spin-on photoresist cannot be used because it causes streaking which leads to problems during exposure. In addition, it does not coat the inside of the vias. Finally, the copper layer is wet etched (Fig. 1e) and the polysilicon is dry etched (Fig. 1f).

Optical micrographs of both sides of the wafer after RIE are shown in Fig. 2. Cross-sectional SEM micrographs of the TWV are shown in Fig. 3.

3. Integrated Three Dimensional Inductor

High performance on-chip inductors facilitate the monolithic integration of systems operating at a frequency between 100 MHz and a few GHz such as wireless communication transceivers [2] and nuclear magnetic resonance detectors [3]. In conventional IC technologies, short via height and large via resistance have limited the form of integrated inductors to a 2D planar spiral.

To demonstrate the performance of this technology, 3D coil inductors are fabricated with the TWV's as the vertical sides of the turns. The front and back sides of a two-turn coil are shown in Fig. 4. Inductance, Q, and series resistance are extracted from measured S_{11} using an HP8720B Network Analyzer and coplanar ground-signal-ground probes. The measurement results are plotted in Fig. 5. A maximum Q of 18.5 is achieved for a 0.9-nH inductor at about 900 MHz. In Fig. 5, the 4-nH inductor has Q greater than 10 at 300 MHz which is a significant improvement over Q of unity obtained with a gold planar spiral on GaAs substrate for the same inductance and frequency [3]. The superior performance of our 3D coils is attributed to the extremely low resistance of the copper interconnects and vias. The resistance of a TWV is extracted from the resistance of the inductors to be less than 50 mΩ.

4. Conclusions

An ultra-low resistance, high wiring density, high yield fabrication technology for through-wafer vias is presented. Using this novel technology, integrated 3D inductors are fabricated that demonstrate high Q.

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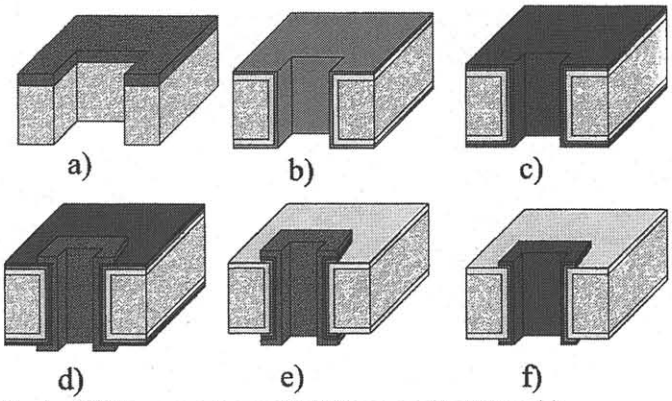

Fig. 1. TWV process flow: a) TWV is dry etched, b) oxide insulation and polysilicon seedlayer are deposited, c) Cu is deposited by CVD and electro-plating, d) photoresist is electroplated and patterned on both sides, e) copper and polysilicon are etched, and f) resist is stripped.

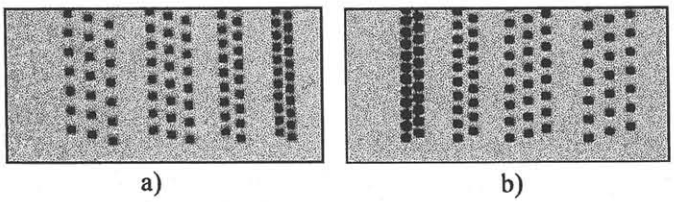

Fig. 2. Optical micrographs of 30-μm wide via arrays with different wiring density: a) front, and b) back sides of the wafer. The wafer is 525 μm thick.

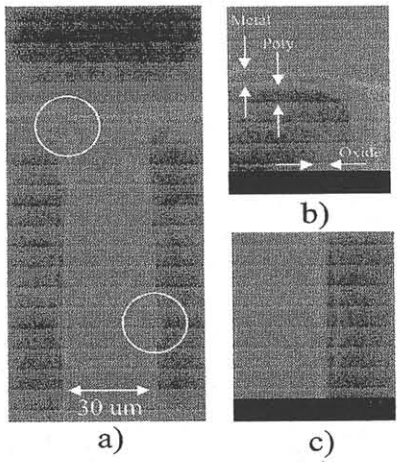

Fig. 3. Cross-sectional SEM micrographs of a TWV. The metallization is 1.5 μm thick for the above sample. a) The via is 30 μm wide and 525 μm deep. Deposited films have good step coverage b) at the corners, and c) on the sidewalls.

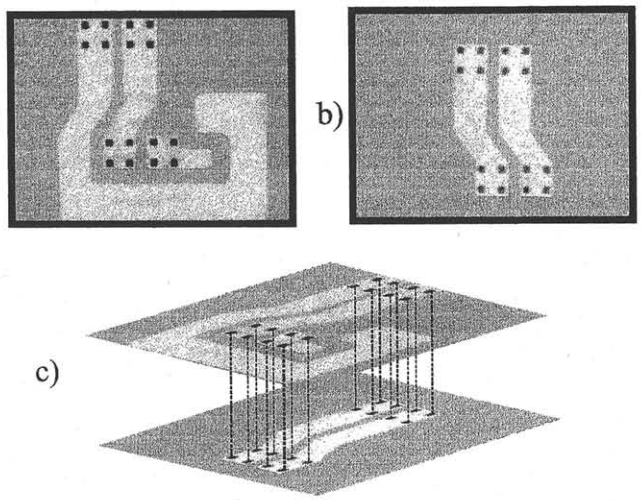

Fig. 4. Optical micrographs of a two-turn inductor with 4 TWV's per vertical connection. Each turn is 500 μm long and 120 μm wide: a) front side, b) back side, and c) 3D rendering of the structure where dotted lines indicate TWV's.

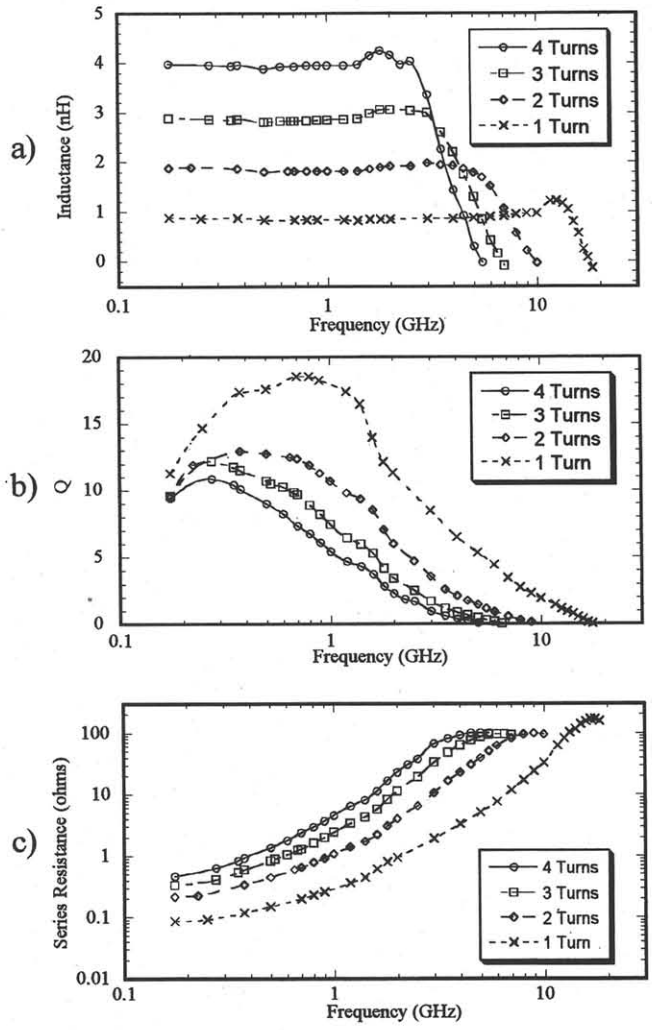

Fig. 5. Electrical characteristics of the integrated 3D inductors as a function of frequency: a) inductance, b) Q, and c) series resistance.