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A New Wafer-Scale Chip-on-Chip (W-COC) Packaging Technology Using Adhesive Injection Method

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1. Introduction

Chip-scale packages(CSPs) offer many advantages over conventional packages due to the reduced size and weight and the improved electrical performance. The demand to further reduction in the package size and the packaging cost is accelerated by portable consumer products like mobile computers, Card PCs and pagers. Thus, low cost and high density packaging technology becomes more important. In order to realize such low cost and high density packaging technology, we propose a new wafer-scale chip-on-chip (W-COC) packaging technology using the adhesive injection method. In W-COC packaging technology, several hundreds of chip-on-chip modules are simultaneously formed in the wafer level. In addition, we can significantly increase the number of vertical interconnections between the bonded two chips by using W- COC packaging since small micro-bumps more than one million can be formed on a chip. Therefore, it is very easy to introduce the parallel processing function in a W- COC module. In this paper, we describe key technologies for such W-COC packaging.

2. Fabrication Process Sequence for Wafer-Level Chip-on-Chip Packaging

In our new W-COC packaging technology, two LSI wafers with many small micro-bumps are bonded in face to face and then the upper wafer is thinned from the back side by the mechanical grinding and chemical-mechanical polishing(CMP). Fabrication process sequence for a chip-on-chip module or a multi-chip-on-chip module using W-COC packaging technology is shown in Fig.1. A 2D LSI wafer is bonded to the other 2D LSI wafer through In/Au micro bumps after careful wafer alignment. The liquid adhesive material is injected into the gap between two wafers in vacuum to enhance the bondability between two wafers. Then, the upper wafer is thinned to around 50 μm from the back side by grinding and CMP. After that, deep silicon trenches are formed through the upper wafer along the periphery of the chip so that the chips on the upper wafer are isolated. Next, the adhesive material exposed at the bottom of trench is removed by O_2 RIE (Reactive Ion Etching). Finally, the lower wafer is cut into the chips by dicing to produce the chip-on-chip module or the multi- chip-on-chip module.

3. Development of Key Technologies for Wafer-Level Chip-on-Chip Packaging

Formation of In/Au micro-bump, wafer alignment, wafer bonding using adhesive injection method, wafer thinning, formation of deep silicon trench and RIE of the adhesive material are the key technologies for W-COC packaging. These key technologies were developed in this work. The process sequence to form In/Au micro-bump is illustrated in Fig.2. The polyimide and the photo-resist are spin- coated and then the via hole is formed through them using O_2 RIE. The In/Au layer is deposited through the photo-resist and the polyimide film. Then, the photo-resist is lifted-off to form the In/Au micro-bump. The SEM micrograph of the micro-bump formed by the lift-off technique is shown in Fig.3. We have developed a new wafer aligner with the alignment tolerance of $\pm$ 1 μm m for the wafer alignment in the wafer bonding using the In/Au micro-bumps. We use the infrared light for the alignment which can pass through Si wafers. In order to enhance the bondability between two bonded wafer, the liquid adhesive is injected into the gap between two wafers. We have developed a new adhesive injection method[1]-[2]. Fig.4 illustrates the insulating epoxy adhesive injection sequence. In this method, an In/Au wall with a small inlet to inject the insulating epoxy adhesive is formed so as to surround the In/Au micro-bump area. Then, the upper wafer is temporary glued to the lower wafer through the In/Au micro bumps and In/Au wall. The temporarily glued wafers are installed in a vacuum chamber which is evacuated to around 10^{-3} Torr. The portion with the small inlet of the temporarily glued wafer is dipped into the insulating epoxy adhesive in vacuum. Then, by changing the vacuum to atmospheric pressure, the epoxy adhesive is injected into the wafer gaps surrounded by In/Au walls because the pressure inside the wafer gaps in the In/Au bump areas is lower than the atmospheric pressure. Fig.5 shows the SEM cross-section of the stacked wafers after injecting the insulating epoxy adhesive. It is clearly shown in the figure that the insulating epoxy adhesive is uniformly filled into the 4μm gap between the stacked two wafers. In order to evaluate the electrical contact characteristics between two micro-bumps in the upper wafer and the lower wafer after injecting the insulating epoxy adhesive, the test model was fabricated. Fig.6 shows the contact resistance characteristics measured using the chain patterns with 40 and 80 In/Au micro-bumps, respectively. Good electrical contact characteristics are obtained. Grinding and chemical-mechanical polishing techniques are used to thin the upper wafer to 50μm. Wafer thickness variation after thinning was as small as 50μm$\pm$ 0.5μm in 6 inch wafer. After thinning the upper wafer, deep silicon trenches are formed through it using ICP (Inductive Coupling Plasma) etching. An SEM cross-section of deep silicon trench is shown in Fig.7. Next, the insulating epoxy adhesive exposed at the bottom of trench should be removed so that the aluminum bonding pads in the lower wafer are exposed. We could remove the insulating epoxy adhesive by using the O_2 RIE with the optimized condition. Using these key technologies developed, we fabricated W-COC test module. Fig.8 shows the photomicrograph of In/Au micro-bumps formed on Al pads in test module. An SEM cross-section of the test module is shown in Fig.9 where it is demonstrated that two chips with the devices are bonded in face to face through the In/Au micro-bumps and the insulating epoxy adhesive. Fig.10 shows an SEM cross-section after forming the deep trench in the upper wafer and O_2 RIE of the exposed insulating epoxy adhesive. It can be seen in the figure that the upper chip is isolated and the exposed insulating epoxy adhesive is completely removed. Thus, we could succeeded in developing the key technologies for W-COC packaging and fabricating a W-COC test module.

4. Conclusion

We have proposed a new wafer-scale chip-on-chip (W-COC) packaging technology using the adhesive injection method. The key technologies for W-COC packaging such as formation of In/Au micro-bump, wafer alignment, wafer bonding using adhesive injection method, wafer thinning, formation of deep silicon trench and RIE of the adhesive material have been developed. In addition, we succeeded in fabricating a W-COC test module.

5. Acknowledgments:

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References

[1] T. Matsumoto et al., Ext. Abstr. SSDM'97, p460 (1997)

[2] M. Koyanagi et al., IEEE CPD'98, p96 (1998)

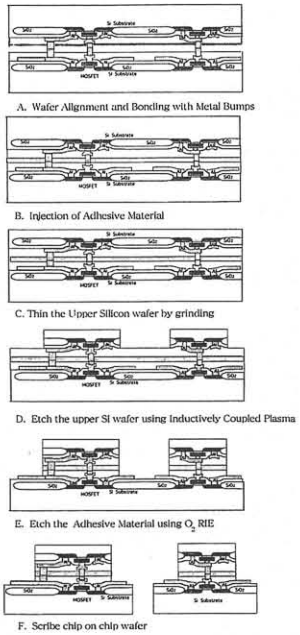


Fig.1 Fabrication sequence for W-COC packaging

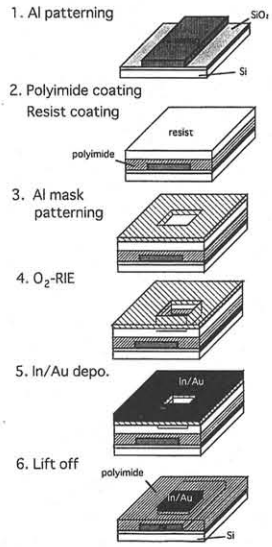


Fig.2 Process sequence to form via hole and In/Au micro-bump.

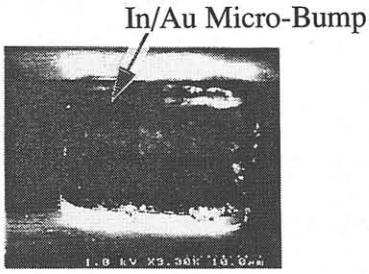


Fig.3 SEM micrograph of In/Au micro-bump.

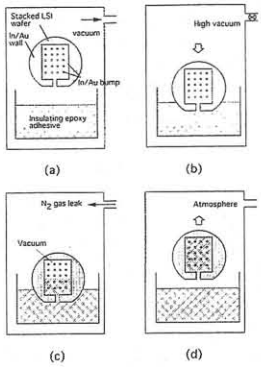


Fig.4 Process sequence of adhesive injection method.

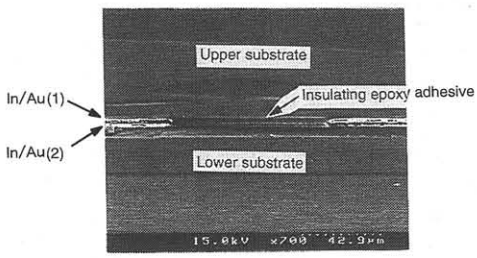


Fig.5 SEM cross-section after bonding two wafers with In/Au micro-bump and injecting the insulating epoxy adhesive.

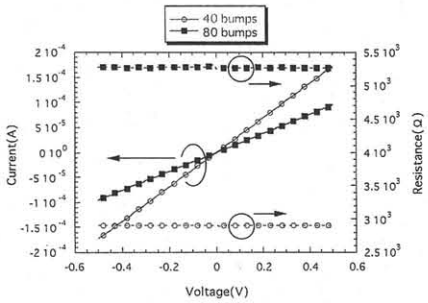


Fig.6 I-V characteristics and contact resistance measured using chain patterns with 40 and 80 In/Au micro-bumps, respectively.

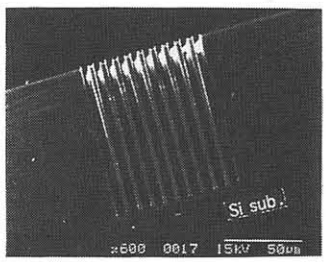


Fig.7 SEM cross-section of deep silicon trench.

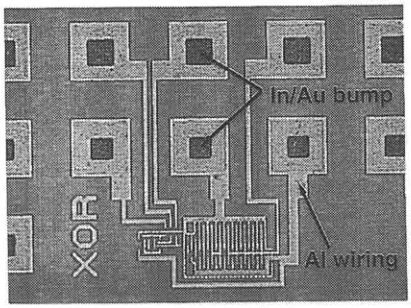
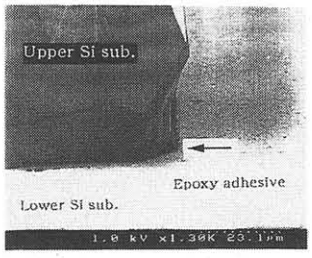


Fig.8 Photomicrograph of In/Au micro-bumps formed on Al patterns in W-COC test module.



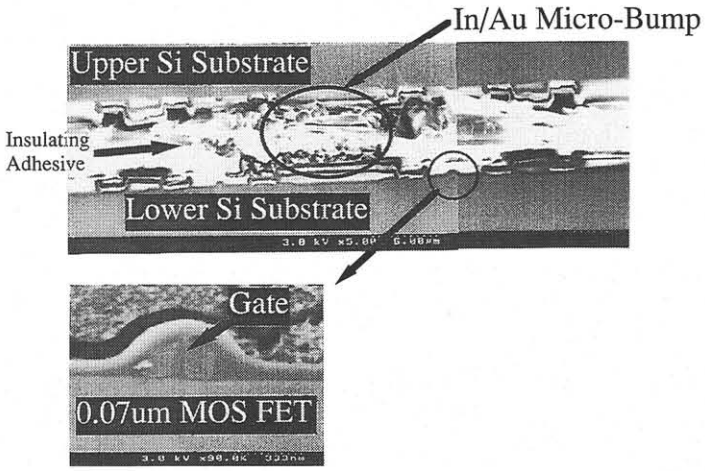


Fig.9 SEM cross-section of the test module.