Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 288-289

Invited

On Shallow Trench Isolation for Deep Submission CMOS Technologies

Amitava Chatterjee, M. Nandakumar, Stan Ashburn, Vikas Gupta, Siang P. Kwok and Ih-Chin Chen†

Silicon Technology Development, Texas Instruments, MS 3702, 13570 N. Central Expressway, Dallas, Texas 75243, USA

1. Introduction- An unabated demand for more integration and higher packing density drives isolation scaling to deca-nanometer dimensions. This paper discusses scaling of Shallow Trench Isolation, *viz,* the issues in lithography; edge leakage; scaling the trench and its effect on stress, latch-up, electrostatic discharge (ESD), CMP, and V_T fluctuations.

2. Lithography- Fig. 1 shows a roadmap for isolation spaces and gate length to support projected circuit densities. The isolation pitch within a well is limited by lithography. In addition, mask overlay becomes critical as the space between an *n* and a *p*MOS shrinks. A constraint for misalignment for the well implant pattern is one-half the n^+-p^+ space. The SIA's projected mask overlay capability (shown in Fig.1) indicates a shrinking process margin. Moreover, the ability to optimize the process is limited since a thick resist is required to block the retrograde well implants. The importance of optimizing the well lithography process is underscored by the observation (Fig. 2 [1]) that even a non-ideal resist profile degrades n^+-p^+ isolation.

3. Edge Leakage- Gate "wraparound" at the trench top edge causes enhanced subthreshold leakage near the active area edges. This results in lower V_T and larger V_T variations at narrow widths (*W*). Most techniques that eliminate this problem also increase width reduction resulting in reduced drive for ultra-narrow devices. These include forming a T-shaped fill either by a short etch to pull back the nitride before trench-fill [2], or by a thin sidewall along the trench edge after nitride strip [3]. Delaying sidewall formation till the pre-gate deglaze shifts the step from active to field area towards the trench [4] solves this problem but possible surface damage and stress raise concerns for GOI. Oxidation processes, tailored to round the top edge [5]-[7], are widely used to reduce the E-field and suppress edge leakage. Of these, high-T RTO gives the smoothest edge [6], [7]. However, oxidation after trench-fill, such as in [7], may cause diode leakage and worsen GOI [6], [8]. Gate oxide growth and gate deposition before trench definition [9], [10] bypasses the problem of exposing the trench edge during pre-gate deglaze has the added complexity of a second gate deposition and etch. A tapered trench etch also prevents edge leakage [11] but scalability is an issue.

4. Scaling the Trench- Fig. 3 shows that shrinking the trench opening has two consequences: the angle θ at which the sidewalls merge gets closer to 90^0; and the aspect ratio of the gap increases. The former limits the trench taper because dislocations are generated by stress during liner oxide growth if the sides taper to a sharp edge at the trench bottom [12]. This forces a trend towards more vertical trenches which also increases stress according to the simulation results [13] reproduced in Fig. 4. It is nontrivial to achieve void-free fill for vertical gaps with an aspect ratio > 4.5 [15]. Reducing the trench depth t_d helps in two ways. It permits more taper before the sidewalls merge, and reduces the aspect ratio. Fig. 4 [13] shows that reducing t_d reduces the peak stress, but its location is then nearer the S/D junctions. Thus, it is more likely to increase diode leakage. Isolation punchthrough voltage and latchup trigger current get worse if t_d is reduced. Fig. 5 shows that both the isolation and latchup performance can be recovered by increasing the well implant dose [15]. Higher dose reduces the well resistances. This affects ESD sensitivity. Fig.6 shows that raising the *p*-well dose degrades the *n*MOS ESD failure current I_{t2}, consistent with the observed correlation between the parasitic bipolar gain of the *n*MOS and I_{t2} [16]. On the other hand, lower well resistances improve ESD failure thresholds in designs that use well diodes to shunt the ESD current [17]. Another consequence of higher well dose is an increased etch rate for the fill oxide, especially for P implants. The resultant excess oxide loss near the trench edge increases the gate "wraparound" and causes a "double hump" in the subthreshold characteristics such as in Fig. 7. Data from a 1Gbit DRAM process [10] show that a 300Å increase in oxide loss results in increased leakage equivalent to a 0.3V lower V_T and introduces large variations at small *W*. Si_3N_4 [18], nitrided SiO_2 [19] and SiO_xN_y [20] trench liners that are used as diffusion barriers to O and B may also help reduce the problem of gate "wraparound".

If CMP uniformity improves then one may reduce the aspect ratio of the gap by thinning the nitride polish-stop layer (Fig. 3). Sensitivity of removal rate to variations in pattern density is the main reason for variations in post-CMP thickness [21]. Methods to improve planarity are shown in Fig. 8, *viz.*, dummy active areas [21], a thin Si_3N_4 overlayer [22] and reverse pattern and etchback, a 2-mask STI process [1]. Fig.9 compares these techniques. Reverse pattern and etch is most effective in reducing $\Delta t_{nitride}$, the difference between post-CMP nitride thickness on a "small" and a "large" active area. Note that reducing t_d results in a smaller $\Delta t_{nitride}$ because the pre-CMP step height is reduced. The step can be eliminated with selective oxide deposition [23] but the liner oxidation after trench-fill is a reliability concern [6], [8].

Isolation using selective epitaxial growth of Si in slots etched into oxide (Fig. 10) is free of the gap-fill problem [24]. Recent success in improving the sidewall electronic quality has revived interest in this scheme [25].

5. V_T Variations- Keyes [26] showed that variations in V_T due to randomness in the number of impurity atoms in the channel have a variance $\sigma^2_{VT} \propto 1/(WL)$. Fig. 11 shows the increase in σ_{VT} with scaling. for the roadmap for oxide capacitance C_{ox} and doping N_{sub} shown in the figure. Dopant fluctuation may not be reduced with better process control. Another fundamental source of variation is the dynamic change in V_T due to electrical coupling with a neighboring node [27]. Simulation results shown in Fig. 12 indicate that this is likely to be unimportant considering the trend towards higher N_{sub}.

Acknowledgement- We thank Drs. M. Rodder, S. Sridhar, A.Amerasekera, C. Duvvury and for their helpful suggestions.

[1] P. Tsui *et al., Symp. VLSI Tech.*, p.152, 1998.
[2] M. Tsai *et al*, US patent 5,712,185, 1998.
[3] P.C. Fazan *et al, IEDM*, p.57, 1993.
[4] T. Ogura *et al., Symp. VLSI Tech*, p.210, 1998.
[5] T. Park *et al., IEDM*, p.675, 1994.
[6] A. Chatterjee *et al., JVSTB*, **15(6)**, p.1936, 1997.
[7] C.P. Chang *et al., IEDM*, p.661, 1997.
[8] H.S. Lee *et al., Symp. VLSI Tech.*, p.158, 1996.
[9] K. Shibahara *et al., IEDM*, p.275, 1992.
[10] J.Alsmeier *et al., Symp VLSI Tech.*, p.19, 1997
[11] K.Ishimaru *et al., Symp VLSI Tech*, p.97, 1994
[12] S. Murtaza, private communication, 1997.
[13] J.Damiano *et al., Symp VLSI Tech.* p.212 1998
[14] M. Nandakumar *et al., IEDM*, p.657, 1997.
[15] S.Murtaza, *et al, Symp VLSI-TSA*, p.113, 1997
[16] A. Amerasekera *et al., IEDM*, p.893, 1996.
[17] S. Voldman *et al., IEDM*, p.811, 1992.
[18] H. Ho *et al.*, US patent 5747866, 1998.
[19] R. Arghavani *et al.*, US patent 5,780,346, 1998.
[20] J.P. Benedict *et al.*, US patent 5,763,315, 1998.
[21] I. Ali *et al, CMP-MIC Conf.*, p.249, 1996.
[22] J.M. Boyd *et al., ECS Proc.*, **95-5**, p.290, 1995.
[23] N. Elbel *et al., Symp VLSI Tech.*, p.208, 1998.
[24] N. Endo *et al., IEEE TED* **ED-31** p.1283, 1984.
[25] J.M. Sherman, *et al., IEEE EDL* **17** p.267 1996.
[26] R.W. Keyes, *J. Appl. Phys*, **8**, p.251, 1975.
[27] J-H Sim, *et al., Symp. VLSI Tech.*, p.32, 1998.

†currently with Worldwide Semiconductor Manufacturing Company, Hsinchu, Taiwan

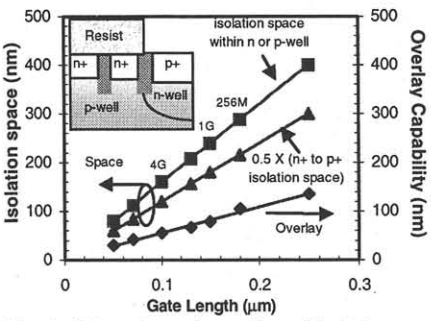

Fig. 1. SIA roadmap for scaling of isolation space and mask overlay capability. Space within *n* or *p* wells is limited by lithography. Space across wells (n^+-p^+) is limited by overlay tolerance.

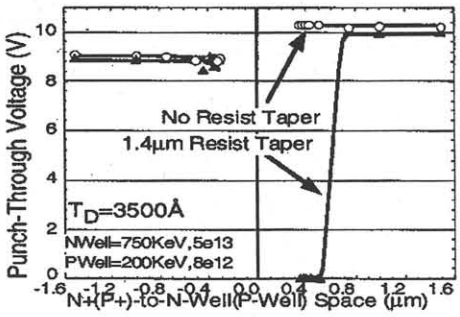

Fig. 2. Interwell (n^+-p^+) isolation is degraded by resist taper for the well implant patterns [1].

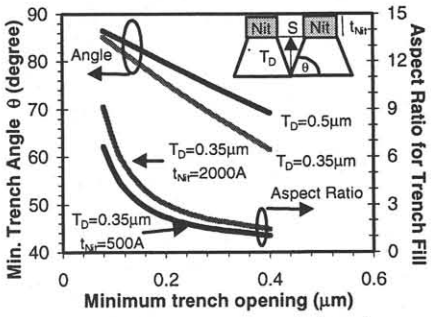

Fig. 3. Minimum trench angle θ and aspect ratio of the gap vs. trench opening.

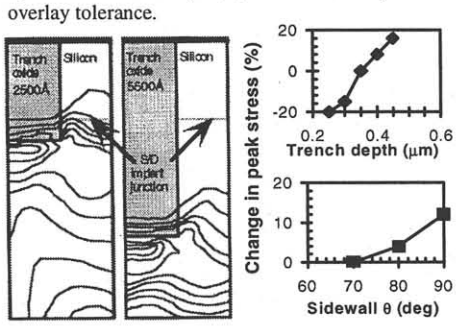

Fig. 4. Simulation of Von-Mises stress due to trench process [13]. More tapered and shallower trenches have less stress. With shallower trenches the peak stress is closer to the S/D junctions, hence more likely to increase diode leakage.

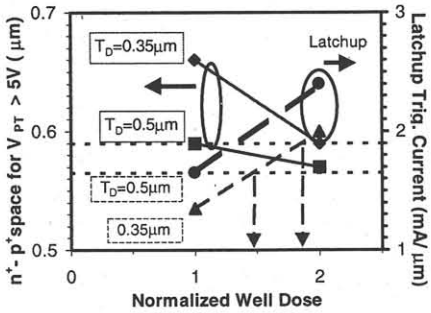

Fig. 5. Interwell (n^+-p^+) isolation and latch-up trigger current vs well dose for two trench depths [15]. Shallower trench needs higher well dose.

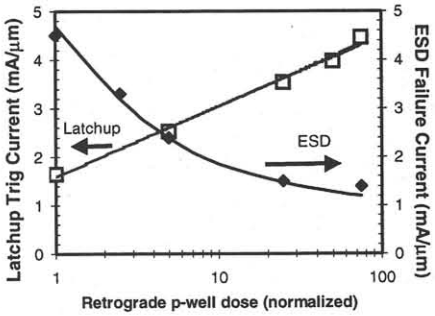

Fig. 6. Tradeoff between CMOS latch-up trigger current and ESD failure current of *n*MOS transistors with increasing *p*-well dose.

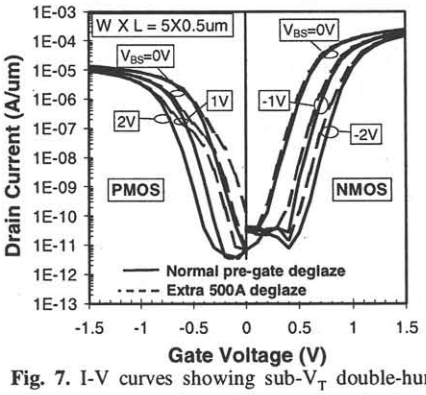

Fig. 7. I-V curves showing sub-V_T double-hump caused by gate wraparound due to excessive loss of oxide around the trench edge at pre-gate deglaze.

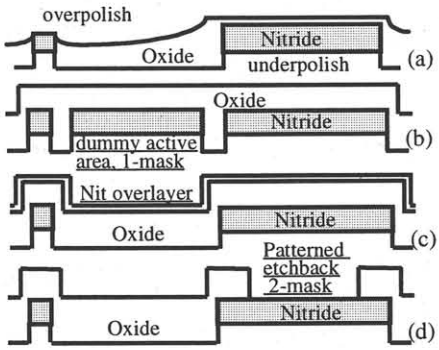

Fig. 8 (a) CMP nonuniformity due to pattern variation (b) Dummy active areas [21], (c) Si_3N_4 overlayer [22], and (d) Reverse pattern and etchback [1]

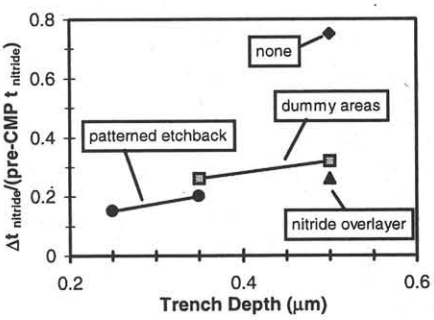

Fig.9 Range of post-CMP Si_3N_4 thickness normalized to the pre-CMP Si_3N_4 thickness vs trench depth compared for various CMP schemes.

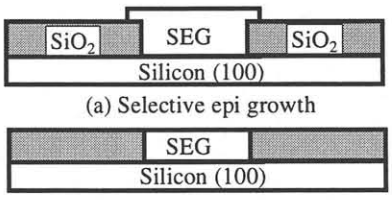

Fig. 10. Isolation scheme using selective epitaxial growth of Si in slots etched in an oxide layer [24], [25] bypasses the problem of filling high aspect ratio gaps.

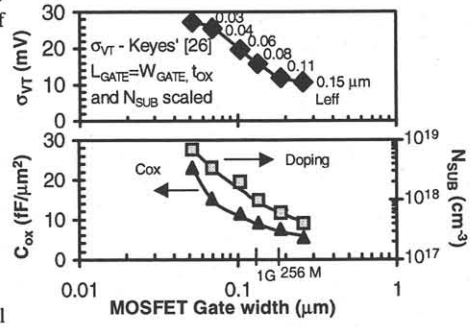

Fig. 11. Variation of V_T due to dopant fluctuation with scaling. Lower plot shows the roadmap used.

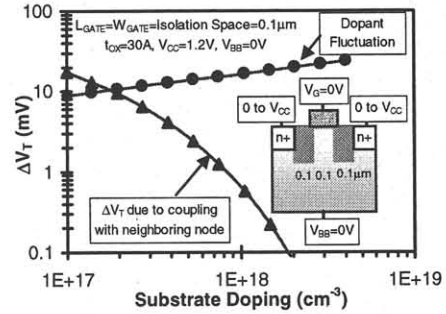

Fig. 12. Simulated dynamic change in V_T due to switching of neighboring node [27] and σ_{VT} due to dopant fluctuation [26] vs substrate doping.