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A Manufacturable HDP Oxide Filled STI Process with SiN Liner for the Deep Sub-Micron Inter-Well Isolation

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Abstract

High Density Plasma (HDP) oxide was examined as the gap filling material of Shallow Trench Isolation (STI). Plasma damage and impurity during the deposition process were analyzed.

Si-defects generated during the STI and the subsequent processes were minimized by effectively suppressing mechanical stress development with the help of a thin SiN film under the HDP oxide.

Introduction

HDP CVD oxide is becoming more widely considered as an STI filling material in deep sub-micron devices [1][2].

However, we are concerned about the application of HDP oxide to STI for the potential danger of the plasma damage and the metallic ion contamination by the high density nature of the plasma.

In the mean time, as shown in Fig. 1, devices which have the HDP oxide filled trenches have shown dislocations accompanying with the short circuited failures and high junction leakage. This suggests that the substrate Si somehow takes heavy stress during and subsequent STI process by the filling of HDP oxide. We investigated the causes of the stress and tried to find a solution to minimize the stress.

Experiments

A. Plasma Damage and Impurity Issues

Plasma damage was indirectly monitored by the measurement of plasma charge voltage in bare wafer. The level of impurity contamination was measured by GF(Graphite Furnace)-AAS and C-V plot before and after bias-temperature stressing.

B. Stress and Defect Issues

Stress hysteresis curves were obtained to see how much stress the Si substrate is experiencing during the densification of the filled HDP oxide. Same analyses were also performed with the O3 TEOS based Undoped Silicate Glass (USG) as a reference. After analyzing the causes of the high defect density with the HDP, we adopted a new structure [3] which has a 5 nm thin SiN liner before the HDP oxide filling. We evaluated device characteristics of this new STI structure. Process conditions regarding STI is summarized in table 1.

Results and Discussion

A. Plasma Damage and Impurity Issues

We performed a preliminary evaluation of the plasma damage of HDP oxide process. Fig. 2 shows that concentric distribution of plasma potential (Vp). The average Vp is 0.496 V and the non-uniformity represented by (Vmax-Vmin) is 0.07V, which is much lower level than that of the conventional dry etching or photoresist ashing. GF-AAS analysis shows that HDP oxide has similar concentration of the elements with USG (Fig. 3), and C-V curve shows no shift before and after stressing in HDP oxide and USG (Fig. 4), which means that there is no significant metal contamination.

B. Stress and Defect Issues

The stress hysteresis of the HDP oxide (Fig.5) shows a much lower peak tensile stress, which can be a cause of defects formation[4], than that of the as-deposited USG. Despite the lower stress level during the thermal cycle, many Si defects have been observed in the STI with HDP oxide.

Fig. 6 and 7 show the transistor off-current and the junction leakage current with the HDP oxide filled STI and the USG filled STI. The transistor off current and junction leakage current with the HDP oxide is higher than that with the USG case, which means more defects are generated in the HDP oxide. However, no defect was detected even with the HDP oxide filled STI in the case that oxidation steps following STI (e.g. sacrificial oxidation and gate etch damage curing oxidation) were skipped. This means that the main cause of defects generation in the HDP oxide is oxidation-induced stress.

Fig. 8 (a) depicts drain saturation current (Idsat) of NMOS transistors with filling materials. The Idsat of the HDP oxide decreased to 93 % compared with the USG, which was due to reduction of active size. Comparing the active size of HDP oxide filled STI with that of the USG filled STI in Fig. 8 (b), the active size of HDP oxide was reduced to about 92 % for USG.

From these results, it is supposed that oxidation rate of the HDP oxide filled STI along the trench sidewall is somewhat higher than that of USG filled STI and hence the active size was reduced more and oxidation-induced defects were generated in STI with the HDP oxide filling. However, it is still uncertain why the oxidation rate increases through HDP oxide. To prevent defect generation, a thin SiN liner was formed as oxidation blocking layer in trench sidewall before HDP oxide deposition. As shown Fig. 9, the transistor off-current was kept in low level and no etch-pit was observed after SECCO etching. Thin SiN liner seemed to effectively suppress further stress generation with the STI sidewall oxidation during the several oxidation steps following STI process.

On the other hand, the distribution of gate oxide breakdown voltage (Fig. 10) shows its best condition with 900 ℃ densification regardless of the liner. It is believed to be because of the smooth profile of gate poly-Si at the trench top corner with the low densification temperature [5].

Conclusions

From the experiments, we showed that plasma damage and impurity level during HDP oxide filling process were low.

The cause of defects formation with the HDP filled STI was higher oxidation rate along the trench sidewall compared with the USG filled STI.

We developed a new STI filling method by adding the SiN liner before the HDP oxide filling, and excellent device characteristics were obtained.

References

[1] S. Nag et al, *IEDM*, p. 841, 1996.
[2] S. Lee et al, *SSDM*, p. 524, 1997.
[3] P. Fahey et al., *U. S. Patent*, No. 5447884, Sep. 1995.
[4] M.H Park et al., *IEDM*, p. 669, 1997.
[5] T. Park et al., *IEDM*, p. 747, 1996.

Fig. 1 Plain SEM view of a device after SECCO etching. Dislocations are seen as etching pit in the field region (Arrows).

Table 1. Process conditions.

Process	Thickness
Pad Oxide	11 nm
Active SiN	250 nm
Trench Depth	600 nm
Trench Sidewall Ox.	24 nm
HDP Oxide	600 nm
PTEOS Oxide	400 nm
Densification	(900 ℃)
CMP	

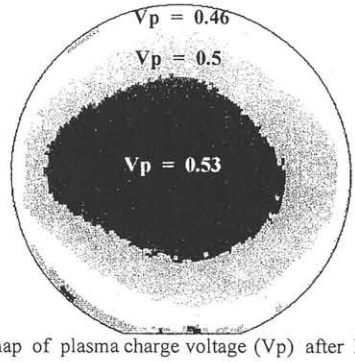


Fig. 2 Wafer map of plasma charge voltage (Vp) after HDP oxide deposition.

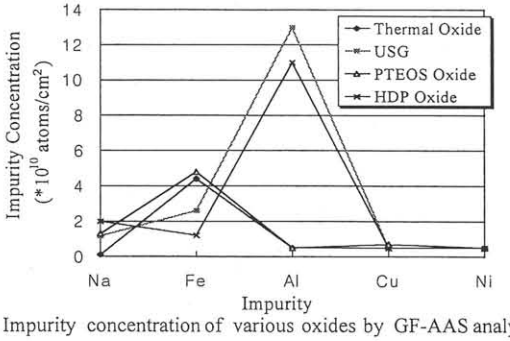


Fig. 3 Impurity concentration of various oxides by GF-AAS analysis.

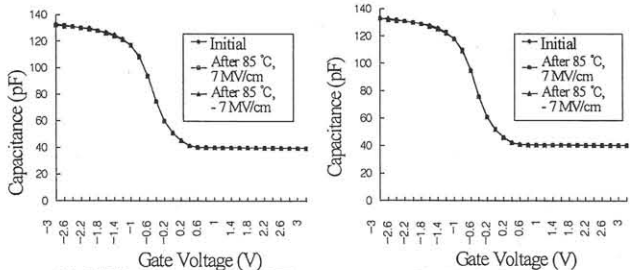


Fig. 4 C-V characteristics after B-T (Bais-Temperature) stressing.

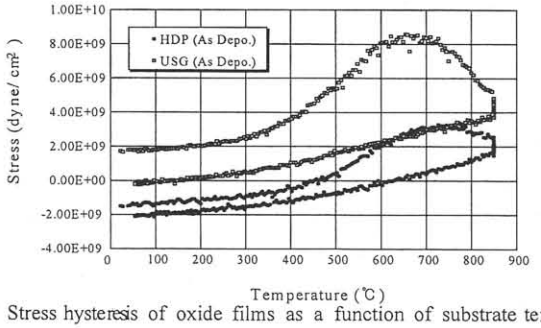


Fig. 5 Stress hysteresis of oxide films as a function of substrate temperature.

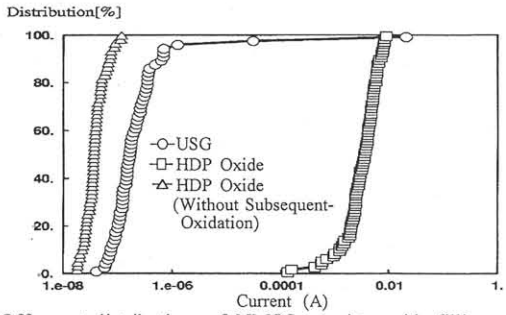


Fig. 6 Off-current distributions of NMOS transistor with filling materials measured at Vd=3.3 V and Vs=Vg=Vb=0 V. (Cell transistor array @300 ea)

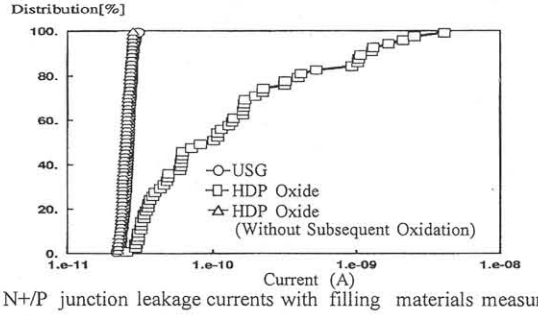
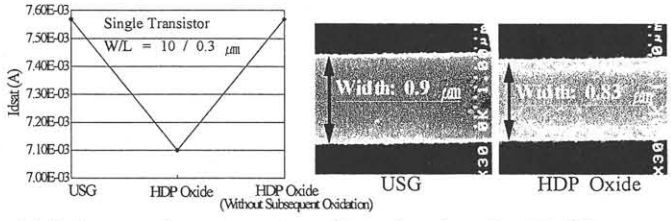


Fig. 7 N+/P junction leakage currents with filling materials measured at 4 V.



(a) Drain saturation current of NMOS transistor measured at Vd=Vg=3.3 V, Vs=Vb=0 V

(b) Active size with STI filling materials. (Original drawing size was 1 μm)

Fig. 8 Drain saturation current of NMOS transistor and active sizes with filling materials.

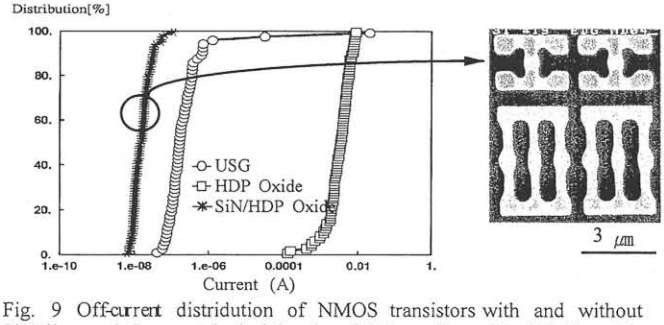


Fig. 9 Off-current distridution of NMOS transistors with and without SiN liner and Secco etched plain view SEM profile with SiN liner. No defect was detected

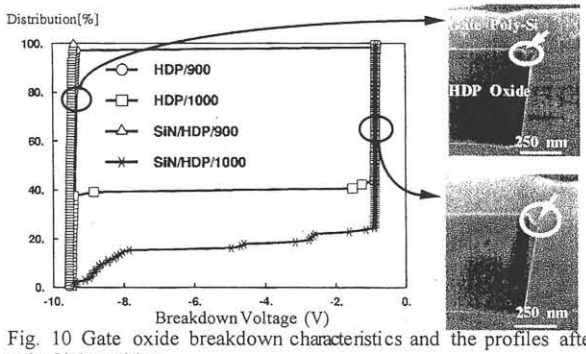


Fig. 10 Gate oxide breakdown characteristics and the profiles after gate poly-Si deposition.