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Facet-Free Si Selective Epitaxial Growth Adaptable to Elevated Source/Drain MOSFETs with Narrow STI

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1. Introduction

An elevated Source/Drain (S/D) has been proposed to achieve shallow junction formation and offer sufficient Si sacrificial layer for Salicide application simultaneously. Si selective epitaxial growth (SEG) is the most promising candidate to form Elevated S/D structure.[1]

However, there are two main issues to be overcome in the SEG process. First, the facet could be formed adjacent to the gate sidewall, which results in the junction leakage.[2] The second issue is that the epitaxial shape on the STI edge, such as facet and lateral overgrowth, is not controllable. Lateral overgrowth will become a degrading factor of the isolation performance of STI in future devices.

The present work proposes a new SEG process which makes facet-free Elevated S/D possible for the MOS application. The novel gate sidewall structure was introduced to suppress the facet formation effectively unless degrading selectivity and planarity of SEG layer. Si lateral overgrowth on STI region was also confirmed to be negligible in this SEG process.

2. Facet-free elevated S/D

The sample fabrication procedure is shown in Figure 1. The novel sidewall structure, SiO_2 liner under SiN sidewall, was used. SEG was performed on this MOS structure with $SiH_2Cl_2/HCl/H_2$ gas mixture using LP-CVD. The typical deposition temperature is 850℃ and the total gas pressure is 10Torr. In-situ H_2 pre-bake was carried out at 850℃ for 3 minutes in order to remove native oxide on the S/D region before SEG.

Figure 2 shows the cross sectional SEM and TEM images of this sample to which the novel elevated S/D technology was adapted. It is clearly demonstrated that facet formation is successfully suppressed. We show as follows that the facet-free elevated S/D formation was realized by the novel SiN/SiO_2 bottom-edge structure.

The key of the facet-free elevated S/D is schematically summarized in figure 3. When epitaxial layer is adjacent to SiO_2, this is the first step of SEG, facet is inevitably formed. On the next step, being adjacent to SiN, epitaxial layer grows freely. In the case of figure 2, the facet is expected to be screened inside the SiN sidewall. Therefore, only the plane surface of epitaxial Si could be adjacent to SiN sidewall and no more facet is formed.

As mentioned above, we effectively utilized the difference of surface affinity between SiO_2 and SiN to realize a facet-free elevated S/D. SiN has better affinity than SiO_2, thus Si nucleates more easily on SiN (figure 4).

In order to investigate the relation between the facet-free properties and the bottom-edge structure of the gate sidewall in detail, the SiN line pattern sample with the SiO_2 liner under SiN were prepared. For the sake of clarify the shape of the bottom-edge, 50nm thick SiO_2 liner was used. Then, the length of side-etch was varied.

In figure 5, the condition of facet formation is demonstrated. The length of the side-etch of the SiO_2 liner under SiN pattern is about 20nm. The {311} facet adjoins the SiN sidewall obviously. Figure 5(a) clearly shows that the facet formed adjacent to SiO_2 liner, and once it was formed, the faceted shape is maintained even when epitaxial growth progresses and facet comes adjacent to SiN sidewall (Figure 5(b)).

Figure 6 shows the facet-free case. In this case, the side-etch length of the SiO_2 liner is about 80nm. It is clear that no facet is observed. This is because the facet was hidden inside the liner SiO_2 etched region.

Facet-free condition is explained in figure 3. It is known that SEG on the (100) wafer result in {311} facet formation adjacent to [110] directioned SiO_2 pattern. Therefore, the condition to suppress the facet formation is subscribed as " $\tan\theta > y/x$ ", where θ is facet angle, x is lateral etch length and y is the thickness of SiO_2 liner respectively. For example, in case of the (100) wafer is used, we could define $\theta = 25.3°$

In this model, the faceted edge is settled to the bottom-edge of liner SiO_2. However, the facet plane grows up during SEG process, in fact. Therefore, this is rather strict condition for facet-free elevated S/D.

3. Lateral overgrowth on the STI

The distribution of lateral overgrowth length normalized by thickness of epitaxial Si is shown in figure 7, and figure 8 shows the cross sectional TEM images of STI after 200nm thick Si selective epitaxial growth. In case of 800℃ SEG, lateral overgrown Si is polycrystalline. However, in case of 850℃ SEG, lateral overgrown Si is single-crystalline. Therefore, the overgrowth controllability is better for 850℃SEG.

From this point, the lateral overgrowth length is controllable by the use of typical facet-free SEG condition at 850℃.

4. Conclusion

Facet-free elevated S/D was realized by means of side-etching of SiO_2 liner. This method could be successfully adapted to the MOS structure with SiN sidewall and SiO_2 liner layer. In this SEG process, also the Si lateral overgrowth and thinning on STI region is confirmed to be negligible.

References

1) J. T. Fitch, *J. Electrochem. Soc.*, **141**, 1046 (1994)
2) C.-P. Chao et al., IEDM-97, 103 (1997)

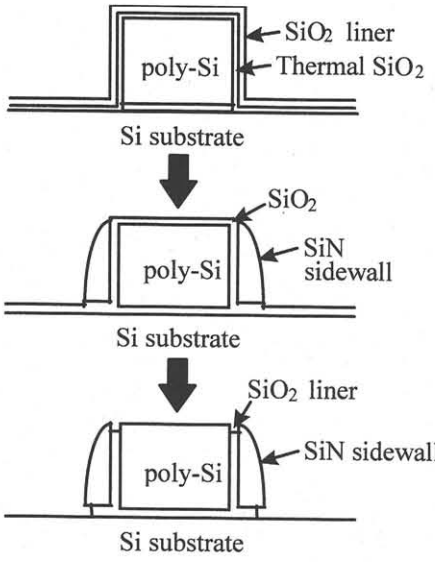


Figure 1.Gate electrode with SiN sidewall sample fabrication procedure

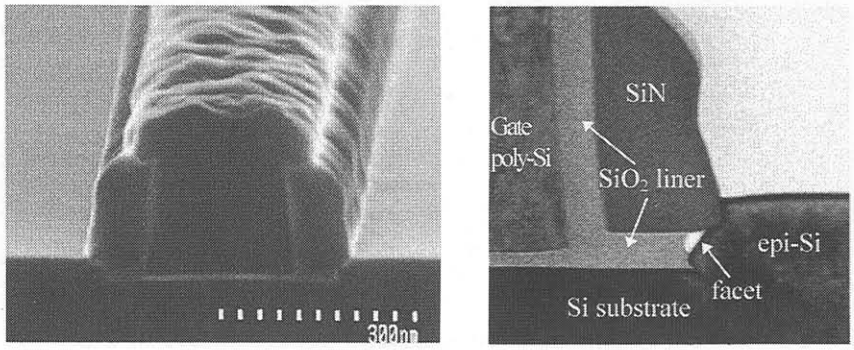
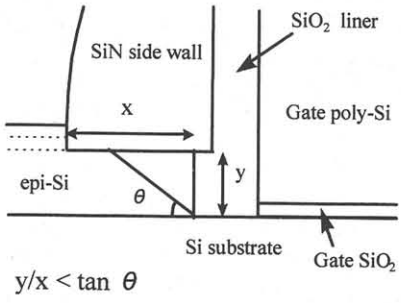


Figure 2. Cross sectional SEM and TEM images of Facet-free elevated S/D



$y/x < \tan\theta$

Figure 3. Facet-free condition to hide facet under the sidewall

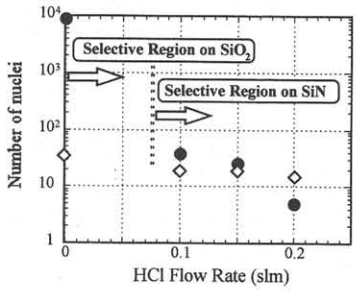
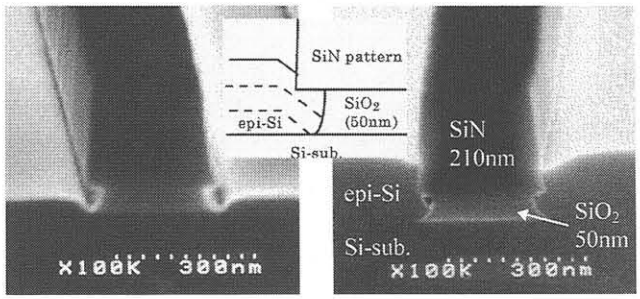


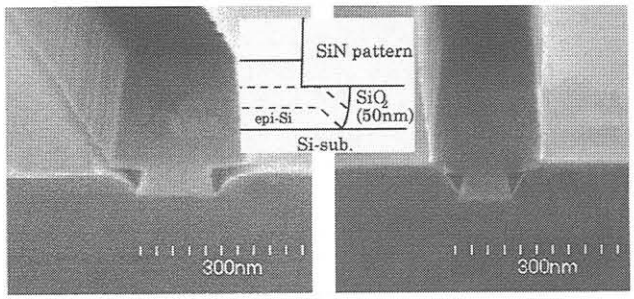
Figure 4. SEG region on SiO_2 and SiN
Number of nuclei for SiO_2(◇) and SiN(●)



(a) Facet formation adjacent to SiO_2 liner

(b) Facet shape is maintained adjacent to SiN

Figure5. SiN pattern after SEG
Facet form condition (20nm side-etch)



(a) Facet formation adjacent to SiO_2 liner

(b) Facet screened under the SiN Planar epi-Si could be fabricated

Figure 6. SiN pattern after SEG
Facet-free condition (80nm side-etch)

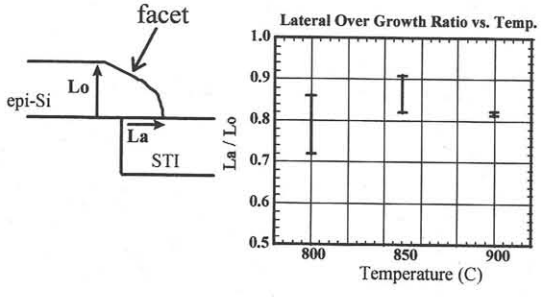
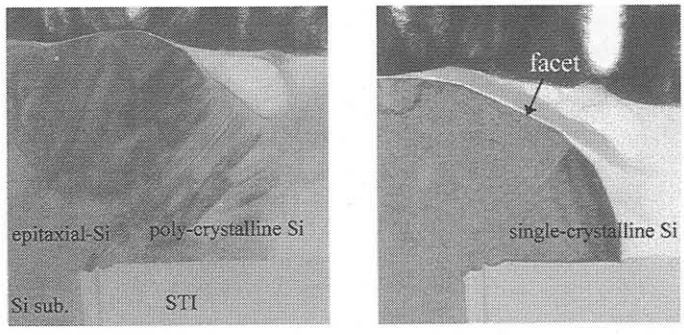


Figure 7. Distribution of overgrowth length normalized by thickness of epitaxial Si



(a) SEG temperature 800C

(b) SEG temperature 850C

Figure 8. Lateral overgrowth on STI