Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 30-31

Implementation of "System On a Chip" Merging DRAM and Analog with High Performance 0.35um Logic Device

Sunil Yu, Jong Shik Yoon, Hyae Ryoung Lee, Chul-Soon Kwon, Dong Woo Kim, Won Chul Kim and Chang-Sik Choi
LSI TD, System LSI Business, Samsung Electronics Co. Ltd.,
San #24 Nongseo-Ri, Kiheung-Eup, Yongin-city, Kyungki-Do, Korea
Phone/FAX : +82-331-209-6589/4399, E-mail: yuandyu@samsung.co.kr

1. Introduction

Since the early 1990s, the semiconductor industry has evolved with the goal of integrating an entire system onto a single die. Specially, Merged DRAM with Logic(MDL) technology has been most widely investigated due to several advantages, such as high on-chip memory band width, low power consumption mainly due to the power reduction in I/O bus buffers driven by DRAM access and customized memory size, low EMI noise due to the less pin counts[1]. Along with MDL process, an integration of analog functionality on a chip is believed to play a key role in the implementation of "system on a chip" in the true sense of the word. Nowadays, a large portion of ASIC designs include analog functionality and its importance in ASIC design are expected to increase more rapidly in the future.

In this work, a process integration of Logic LSI merged with DRAM and analog using high performance 0.35μm CMOS and Metal-Insulator-Metal(MIM) capacitor technology is described.

2. Results and Discussion

DRAM Related Process

The key process feature of this study was that the aluminum alloy layer was used as a bit line in DRAM cells on the contrary to the employment of polycide in the conventional DRAM technology. The metal bit lines in DRAM core were shared with 1st level metal in the logic part to simplify the process steps and reduce mask layer. The typical cross sectional views of DRAM cell area and logic part prepared in this work are shown in Fig. 1. The cell size of DRAM produced was 2.1μm^2. Triple well type was introduced to bias P-well in which DRAM cell was fabricated independently from the other logic and analog area. P-well in DRAM cell area was separated from P-sub by building it above deep N-well and by surrounding side wall using N-well. Modified Polysilicon Spacer LOCOS (PSL)[2] technique was employed for the field isolation. The channel stop implantation, as-grown field oxide thickness, sacrificial oxidation and subsequent removal step and related wet treating process had to be well optimized to guarantee the small active opening necessary for the formation of DRAM cell in the most compact area in DRAM core region suppressing extended bird's beak penetration effect as well as good field isolation characteristics at narrow active space as low as 0.5μm.

Logic Process and Transistor Performance

It is very essential to keep transistor performance as high as standard logic ones to benefit fully from the integration of logic and DRAM on a chip. In this study, source and drain region were fabricated after high-temperature capacitor process. The process parameters and process architecture were optimized to keep the high performance of transistor characteristics in spite of the additional thermal budget due to the formation of storage capacitors. Ti-silicide layers on N+ and P+ active area of logic circuitry were prepared employing the conventional silicide process, whereas the active area in DRAM cells was kept from silicidation using by silicide blocking layer during silicide process. The typical values of Idsat of NMOS/PMOS transistors obtained in this work were about 530 and 250μA/μm at 3.3V, respectively. The typical plots of drain current vs. drain voltage at various gate bias condition for NMOS and PMOS are presented in Fig. 2. The drain leakage currents for both type of transistors at 0V of gate bias and 3.6V of drain voltage were in the range of 10^{-13}A/μm. NMOS and PMOS transistors did not show any significant reduction in their threshold voltage due to the short channel effect up to the point of 0.35μm gate length (Fig. 3).

Dual gate oxide process was developed to support 5 volt operation as well as 3.3volt adding one more mask to normal 3.3volt process. As-grown gate oxide thickness of 3.3volt operation transistor was 70Å, while the gate oxide thickness of 5volt transistor was 117Å. It was possible to control the gate oxide thickness of the high voltage transistor within ±1.5Å on 6" wafer by optimizing wet cleaning process.

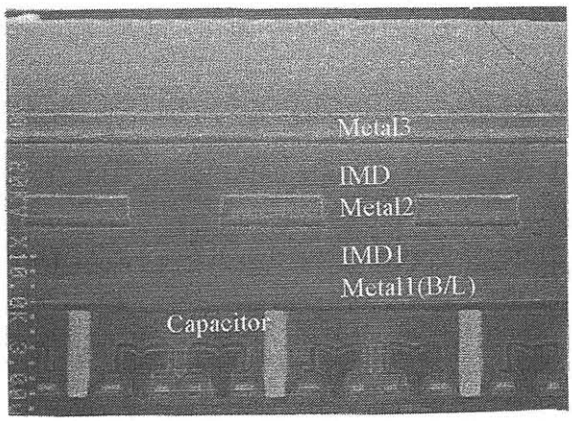
Analog Process

In this study, MIM capacitor instead of conventional Poly-Insulator-Poly (PIP) was used to improve the VCC (voltage coefficient of capacitance) characteristics for the application of high resolution analog cores. Tungsten was used as a top electrode of MIM capacitor while the bottom electrode was aluminum(Fig. 4). The value of capacitance was 0.55pF/μm^2. The value of VCC far less than 50ppm/V was obtained with good matching characteristics (Fig. 5).

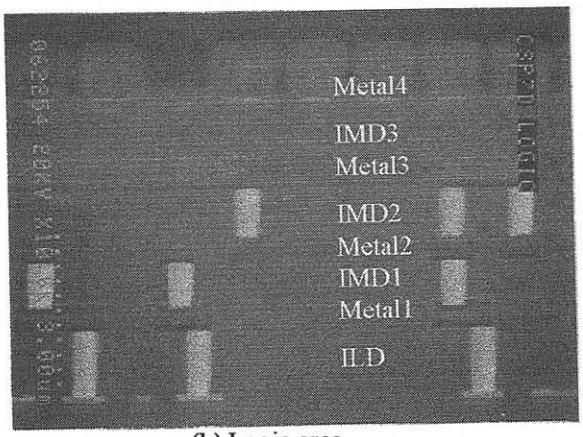
3. Conclusions

In this work, DRAM and analog were successfully embedded in high performance 0.35μm logic chip, supporting 5volt operation as well as 3.3volt. The typical

values of Idsat of NMOS/PMOS transistors were about 530 and 250μA/μm at 3.3V, respectively. The low value of VCC of analog capacitor (less than 50ppm/V) was achieved employing MIM capacitor process. Recently, the process has been proven by successful implementation of scanner one chip composed of 1M DRAM core, AFE analog core, MPU core and DSP core.



(a) DRAM cell area



(b) Logic area

Fig. 1 Cross sectional views of DRAM cell and logic area

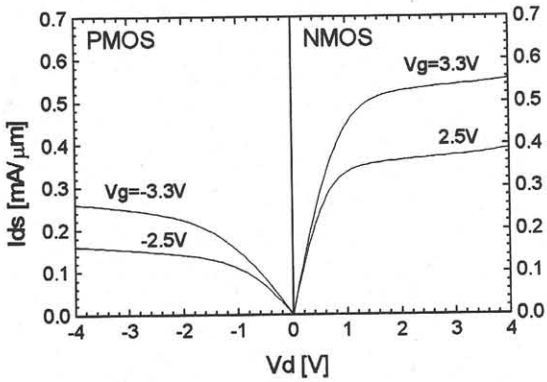


Fig. 2 I-V characteristics for 0.35μm NMOS and PMOS with 530 and 250μA/μm driving currents at 3.3V, respectively

References

1) S. Kawamura, Merged Memory & Logic Process /Device Technologies, in Proc. SEMICON Kansai 97 ULSI Technology Seminar, May 29-30, 1997, 2-30

2) D. H. Ahn et al., A Highly Practical Modified LOCOS Isolation Technology for the 256 Mbit DRAM, IDEM Tech. Dig., p679, 1994

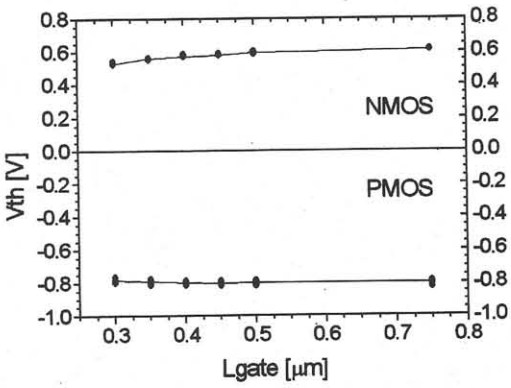


Fig. 3 Threshold voltage vs gate length

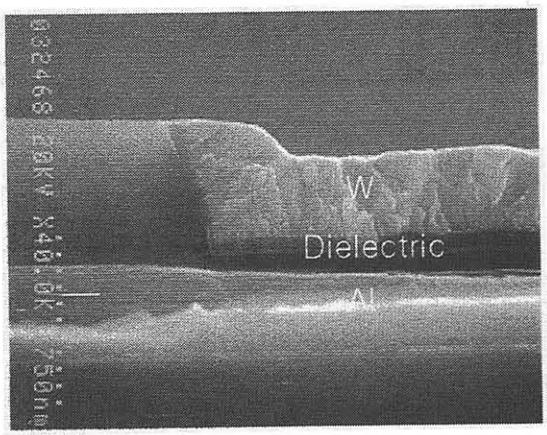


Fig. 4 Cross sectional view of MIM capacitor

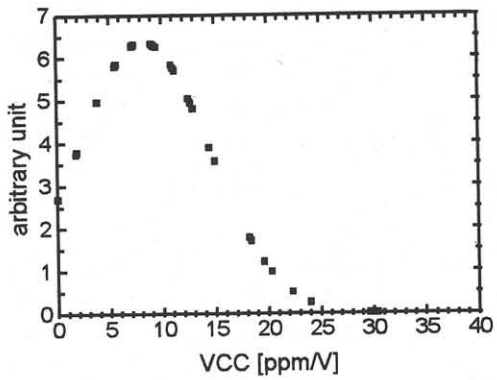


Fig. 5 Distribution of VCC(voltage coefficient of capacitance) for MIM capacitor