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Trap Assisted Leakage Mechanism of 'worst' Junction in Giga-bit DRAM Using Negative Word-Line Voltage

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1. INTRODUCTION

For maintaining refresh performance of Gbit DRAMs, the reduction of leakage current, and more essentially, specification of the leakage mechanism[1] at the worst bit are considered to be substantially important. The junction leakage is one of the dominant factor of the leakage, which has been widely investigated, but usually only the average value of leakage was discussed.

Recently, application of negative gate bias has been reported[2] as a promising technology for Giga-bit DRAMs. However, this negative bias increases the electric field between the gate and the drain. It leads to another leakage mechanism, such as a band-to-band (BTB) tunneling[3].

In this report, we will describe the specification of the conduction mechanism at 'worst' junction under negative gate bias.

2. EXPERIMENTS

The test structure for this experiment is drawn in Fig.1. nMOSFETs with 4nm gate oxide and LDD structure were fabricated. RTA treatment was applied after As-LDD implant. RTA process was conducted at the temperature of 1000℃ for 10sec, and the ramping rate was 250℃ /sec. The leakage current was measured for 490 drain junctions on the same wafer with different gate bias(Vg) and substrate bias(Vsub).

3. RESULTS AND DISCUSSION

The typical deviation of the leakage current for 490 junctions is shown in Fig.2. The horizontal axis is plotted with the inverse of leakage current, assumed to be equivalent to the retention time. For the following analysis, 3 groups of the junctions, as the worst, best, and average samples, were extracted from these devices.

The dependence on the temperature was examined for the each of them, and the results are shown in Fig.3. At Vg=0 (Fig.3(a)), the activation energy (Ea) at 80℃ for all samples were nearly 0.5eV, which suggests the dominant conduction mechanism is the generation from the depletion region. In this bias condition, the worst junctions exhibit larger leakage current, but the dependence on the temperature were almost the same as the other groups. It is supposed that larger leakage current in 'worst' junctions suffers from the generation current due to relatively high trap density in the depletion region, and, however, the leakage mechanism is the same as 'average' and 'best' junctions. When the negative Vg was applied (Fig.3(b)), the 'worst' junctions clearly shows distinctive characteristics.

The changing of the electric field by negative Vg application was evaluated with 2D device simulations. The typical profile of electric field was shown in Fig.4, and the maximum electric field (Emax) for different bias conditions were listed in Table 1. When negative Vg was applied, Emax dramatically enhanced, but the changing of Vsub does not affect to Emax. This enhancement of the electric filed is supposed to be a reason for 'worst' junctions. As shown in Fig.4, the Emax was observed at the surface of LDD region overlapped with the gate electrode.

The dependence of Ea on the bias voltage are described in Fig.5. When negative Vg was applied, Ea of 'worst' junctions indicate larger reduction, as shown in Fig.5(a). This lower Ea means tunneling mechanism. From above results, we can conclude that the trap assisted tunneling mechanism under high electric field is the main cause of large leakage current of 'worst' junctions with negative gate bias.

Ea was reduced by increasing negative Vg bias, but it was independent of Vsub, as shown in Fig.5(b). This phenomena corresponds to Emax dependence on bias condition, as described before. It means the location of these traps should be restricted to the surface of the LDD region overlapped with the gate electrode.

4. CONCLUTIONS

We have demonstrated that the characteristics of 'worst' junctions was specified by the trap assisted tunneling at the LDD region overlapped with the gate electrode under the negative Vg conditions, and this brings about large deviation of junction leakage current. This mechanism must be carefully considered when designing giga-bit DRAM cell transistors utilizing negative word-line scheme.

REFERENCES

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3) M.J.Chen, H.T.Huang, C.S.Hou, and K.N.Yang, IEEE EDL, Vol.19, No.4, Apr 1998, p.134-136

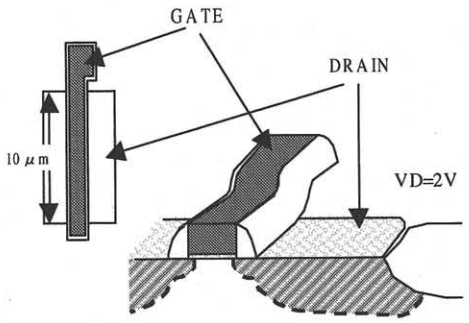

Figure 1
The structure of the measured sample.

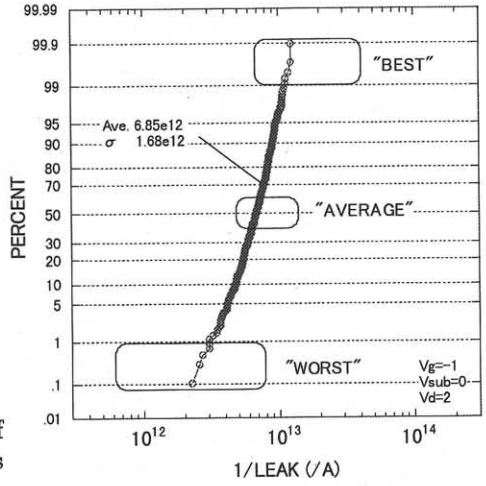

Figure 2 The typical distribution of leakage current for 490 junctions. 3 gorups were extracted for analysis.

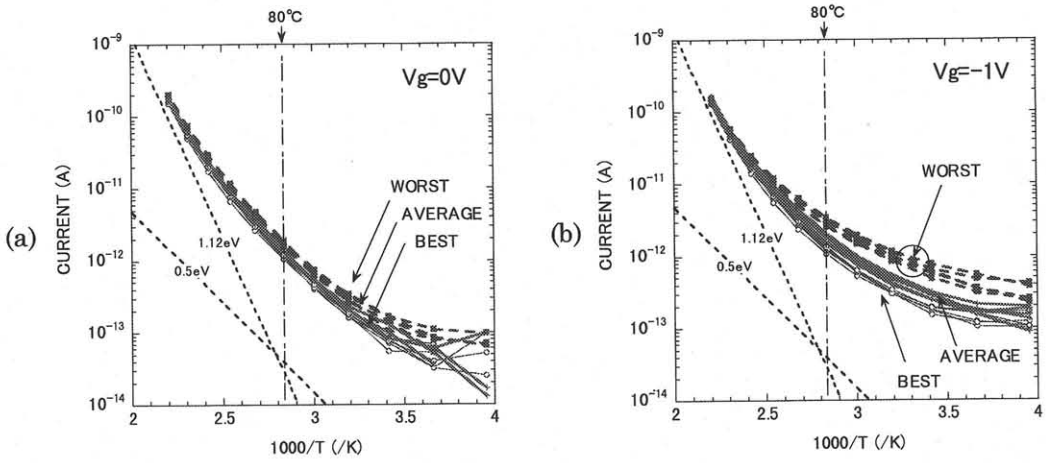

Figure 3 The leakage dependence on the temperature for each groups, shown in fig.2. Different Vg was applied, Vg=0V in fig.3(a), and –1V in fig3.(b).

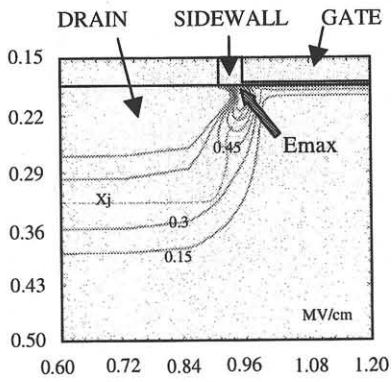

Figure 4
The simulated profile of the electric field, when negative Vg was applied. Vg=Vsub=-1.

Table 1
The maximum electric field (Emax) for various bias condition.

Vg	-1V	-1V	0V
Vsub	-1V	0V	-1V
Emax (MV/cm)	1.31	1.32	0.98

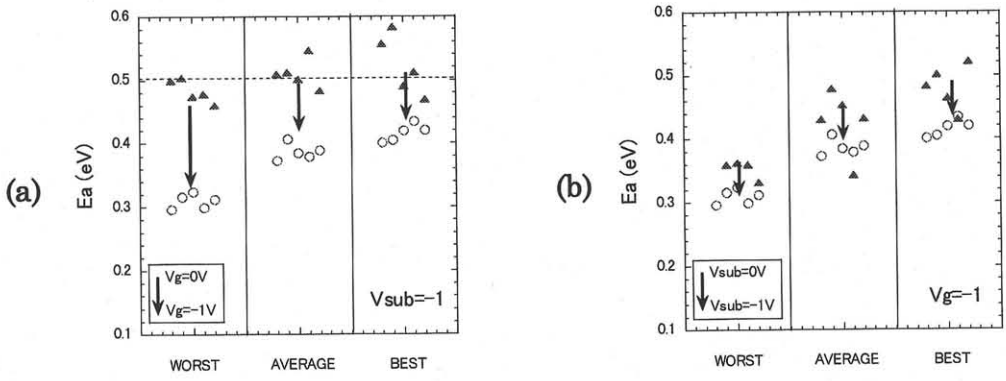

Figure 5 The activation energy dependence on the bias condition for 3 groups of junctions. The distinctive reduction of Ea under negative Vg was observed for 'worst' junctions.