An Analytical Delay Model for Read Operation at Any Position on DRAM Bit Lines

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1. Introduction
As devices shrink to deep submicron or below, the interconnect effects are getting more significant, thus the gates and interconnect had better to be combined and modeled as a single component. Unlike traditional approaches, people concentrated on either CMOS gates [1] individually or transmission lines that are modeled as distributed RLC [2] or RLG [3] networks. In this paper, the analytical delay model at any positions on DRAM bit lines with any initial voltages in read operation is derived. The excellent agreement between the new model and the Spice simulation using BSIM3 model is also demonstrated.

The geometry of 1-bit dynamic random access memory (DRAM) cell and the equivalent circuit is illustrated in Fig. 1. The DRAM cell is composed of a capacitor \( C_{\text{data}} \) which stores the data, a 3.3V/0.35μm N-MOSFET with a word line to control the switch and a long bit line that is usually made of polysilicon. When the data is read out, the signal needs to go through the bit line and reach the sense amplifier, which is modeled as a capacitor \( C_i \) as shown in Fig. 1. \( C_m \) is the FET source junction capacitance plus \( C_{\text{gs}} \). The bit line with length of \( L \) is modeled as distributed RC circuits. The total resistance and capacitance of the bit line are \( R \) and \( C \), which mean the resistance/length and capacitance/length can be expressed as \( R = \frac{R}{L} \) and \( C = \frac{C}{L} \), where \( C = C_{\text{mos}, \text{cell}} \cdot n + C_n \) in which \( C_{\text{mos}, \text{cell}} \) is the junction capacitance of MOSFET; \( n \) is the number of bit cells along the bit line; \( C_n \) is the capacitance of the bit line.

![Fig. 1 The cross section and equivalent circuit of a DRAM cell](image)

2. The analytical model
To derive the analytical approximated delay model for read operation in deep submicron DRAM cells with long and narrow polysilicon bit lines, the similar technique to find the delay for an inverter driving a capacitor load through a long wire [4] was applied. Unlike Ref. [4], the inverter was replaced by a DRAM cell as proposed in Ref. [5]. Instead of using a simple resistor to model an N-MOSFET, the saturation current equation proposed in Ref. [6] for the CMOS gate delay was adopted.

Since the initial value of \( C_{\text{data}} \) is 3.3V and that of the other capacitors is higher than or equal to 0, the N-MOSFET should be in saturation regions after the word line ramps to higher voltages. Once the FET turns on, \( C_{\text{data}} \) starts to discharge and the current through the FET \( (I_{\text{data}}) \) is the sum of the current through the bit line and \( C_m \) dv/dt.

\[
I_{\text{data}} = I_D - G_m V_2
\]

where \( I_D \) and \( G_m \) are functions of \( V_s, V_{\text{th}} \), channel length and width, mobility and initial voltage on the bit line \( (V_{\text{in}}) \). By converting \( V_s, V_2 \) and \( I_{\text{data}} \) into Laplace transforms, while employing the similar technique in Ref. [4], the analytical voltage expression at any point on the bit line is obtained, where \( x \) is the distance from the sense amplifier. The coefficients \( \delta_i \) and \( C_i \) are given below.

\[
\tan \sqrt{\delta_i} = \frac{\Gamma - (C_M + C_U)}{R} \delta_i
\]

\[
C_i = \frac{2RI_{\infty}^2}{P_{\infty} \cos \frac{\sqrt{\delta_i}}{2} - P_{\delta} \cos \frac{\sqrt{\delta_i}}{2}}
\]

where \( \delta = R \alpha \), \( C_1 = C_2 \), \( C_M = C_m \) and \( P_{\infty} = 2 \delta - \delta_1 \Gamma - 4 \delta_1 C_M + C_L \Gamma + C_M C_L \delta_1 \gamma \), \( P_{\delta} = 2 \Gamma - \delta_1 \Gamma - 4 \delta_1 C_M + C_L \Gamma + C_M C_L \delta_1 \gamma \)

Fig. 2. Waveform of a typical bit line at any position when using Spice simulations.

Even though the solution is an infinite series, the first exponential term is usually dominated. Thus, only the term of \( k=1 \) was used in the following evaluation unless specified.

3. Evaluation of the model
To evaluate the accuracy of the new analytical model, transient simulation of the DRAM cell as shown in Fig. 1. using Spice with the BSIM3 model of 0.35μm N-MOSFET's was performed. In the following figures, the standard conditions are \( C_{\text{data}}=50/F, C_C=120/F, C_I=80/F, R_A=700\Omega, \) and \( W=0.5\mu m, V_{\text{in}}=0, \) and \( V_{\infty}=V(t,0) \) unless specified in the figures. Figs. 2, 4, 5 and 6 demonstrate excellent agreement of \( V_s \) (solid lines) between the new analytical model and the simulation (dotted lines). In Fig. 2(a), the final steady state voltages \( (V_s) \) are 0.664V and 0.452V for \( C=120/F \) and 240/F, respectively. \( R=33\Omega \) and 700Ω are equivalent to aluminum and polysilicon bit lines. In Fig. 2(b), \( V_s \)'s are 0.664V and 0.392V for \( C=80/F \) and 250/F. It can be observed that when...
$V_o$ is close to $V_n$, the new model starts to deviate from the simulation due to the invalid assumption of the FET to be in saturation.

![Figure 2(a) $V_o$ vs. $t$ for different $R$ and $C$](image)

![Figure 2(b) $V_o$ vs. $t$ for different $W$ and $C_t$](image)

Fig. 2(a) $V_o$ vs. $t$ for different $R$ and $C$.

Fig. 2(b) $V_o$ vs. $t$ for different $W$ and $C_t$.

Fig. 3 demonstrates the percentage error in time domain for given $V_o$'s in terms of percentage of $V_f$ for various values of $R$, $C$ and $C_t$. In general, all the errors are less than 4% up to 70% of $V_f$ at $V_o$. The error at higher $V_o$ is due to the FET entering linear regions.

![Figure 3 Error in time domain](image)

4. Conclusions

The new analytical delay model for read operation at any locations on DRAM bit lines has been derived. The accuracy is very good for all reasonable resistance, capacitance and initial voltages on the bit line as well as different widths of N-MOSFETs. This new model will be the quick solution for optimization of DRAM circuits and can also be applied to a transmission gate driving another gate through a long wire.

![Figure 4 $t_d$ vs. $C$ or $C_t$](image)

![Figure 5 $V_o$ for different $V_{in}$](image)

![Figure 6 $V_o$ at different positions](image)

Fig. 4 $t_d$ vs. $C$ or $C_t$.

Fig. 5 $V_o$ for different $V_{in}$.

Fig. 6 $V_o$ at different positions.

References