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An Analytical Delay Model for Read Operation at Any Position on DRAM Bit Lines

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1. Introduction

As devices shrink to deep submicron or below, the interconnect effects are getting more significant, thus the gates and interconnect had better to be combined and modeled as a single component. Unlike traditional approaches, people concentrated on either CMOS gates [1] individually or transmission lines that are modeled as distributed RLC [2] or RLGC [3] networks. In this paper, the analytical delay model at any positions on DRAM bit lines with any initial voltages in read operation is derived. The excellent agreement between the new model and the Spice simulation using BSIM3 models is also demonstrated.

The geometry of 1-bit dynamic random access memory (DRAM) cell and the equivalent circuit is illustrated in Fig. 1. The DRAM cell is composed of a capacitor C_{data} which stores the data, a 3.3V/0.35μm N-MOSFET with a word line to control the switch and a long bit line that is usually made of polysilicon. When the data is read out, the signal needs to go through the bit line and reach the sense amplifier, which is modeled as a capacitor C_l as shown in Fig. 1. C_m is the FET source junction capacitance plus C_{gs}. The bit line with length of L is modeled as distributed RC circuits. The total resistance and capacitance of the bit line are R and C, which mean the resistance/length and capacitance/length ca be expressed as $R_u=R/L$ and $C_u=C/L$, where $C=C_{jNMOS\_cell}\cdot n+C_w$ in which C_{jNMOS_cell} is the junction capacitance of MOSFET; n is the number of bit cells along the bit line; C_w is the capacitance of the bit line.

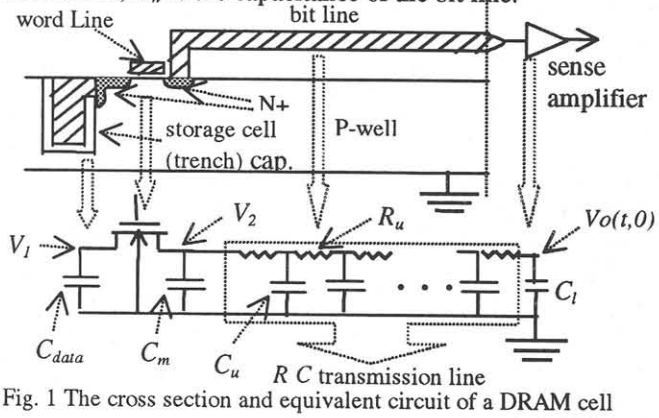

Fig. 1 The cross section and equivalent circuit of a DRAM cell

2. The analytical model

To derive the analytical approximated delay model for read operation in deep submicron DRAM cells with long and narrow polysilicon bit lines, the similar technique to find the delay for an inverter driving a capacitor load through a long wire [4] was applied. Unlike Ref. [4], the inverter was replaced by a DRAM cell as proposed in Ref. [5]. Instead of using a simple resistor to model an N-MOSFET, the saturation current equation proposed in Ref. [6] for the CMOS gate delay model was adopted

Since the initial value of C_{data} is 3.3V and that of the other capacitors is higher than or equal to 0, the N-MOSFET should be in saturation regions after the word line ramps to higher voltages. Once the FET turns on, C_{data} starts to discharge and the current through the FET (I_{dsato}) is the sum of the current through the bit line and $C_m\, dV_2/dt$.

$$I_{dsato} = I_D - G_m V_2 \tag{1}$$

where I_D and G_m are functions of V_g, V_{th}, C_{ox}, channel length and width, mobility and initial voltage on the bit line (V_{ini}). By converting V_2, V_o and I_{dsato} into Laplace transforms, while employing the similar technique in Ref. [4], the analytical voltage expression at any point on the bit line is obtained, where x is the distance from the sense amplifier.

$$V_o(t,x) = V_{ini} + \frac{I_D}{G_m} + \sum_{k=1}^{\infty} C_k \exp\left(-\frac{\delta_k t}{RC}\right) \tag{2}$$

The coefficients δ_k and C_k are given below.

$$\tan\sqrt{\delta_k} = \frac{\Gamma - (C_L + C_M)\delta_k}{(1 + C_L\Gamma - C_M C_L \delta_k)\sqrt{\delta_k}} \tag{3}$$

$$C_k = \frac{2RI_D\left[\cos\left(\sqrt{\delta_k}\,x/L\right) - C_L\sqrt{\delta_k}\sin\left(\sqrt{\delta_k}\,x/L\right)\right]}{P_1\cos\left(\sqrt{\delta_k}\right) - P_2\sqrt{\delta_k}\sin\left(\sqrt{\delta_k}\right)} \tag{4}$$

where $\Gamma=RG_m$; $C_L = C_l/C$; $C_M = C_m/C$; and

$P_1 = 2\Gamma - \delta_k(1 + C_L\Gamma) - 4\delta_k(C_M + C_L) + C_M C_L \delta_k^2$

$P_2 = \Gamma + 3(1 + C_L\Gamma) - \delta_k(C_M + C_L) - 5C_M C_L \delta_k$

Even though the solution is an infinite series, the first exponential term is usually dominated. Thus, only the term of k=1 was used in the following evaluation unless specified.

3. Evaluation of the model

To evaluate the accuracy of the new analytical model, transient simulation of the DRAM cell as shown in Fig. 1. using Spice with the BSIM3 model of 0.35μm N-MOSFET's was performed. In the following figures, the standard conditions are C_{data}=50fF, C=120fF, C_l =80fF, R=700Ω, and W=0.5μm, V_{ini}=0, and $V_o \equiv V_o(t,0)$ unless specified in the figures. Figs. 2, 4, 5 and 6 demonstrate excellent agreement of V_o (solid lines) between the new analytical model and the simulation (dotted lines). In Fig. 2(a), the final steady state voltages (V_f) are 0.664V and 0.452V for C=120fF and 240fF, respectively. R=33Ω and 700Ω are equivalent to aluminum and polysilicon bit lines. In Fig. 2(b), V_f 's are 0.664V and 0.392V for C_l=80fF and 250fF. It can be observed that when

V_o is close to V_f, the new model starts to deviate from the simulation due to the invalid assumption of the FET to be in saturation.

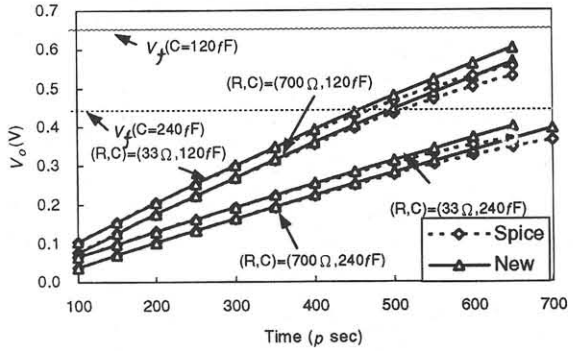

Fig. 2 (a) V_o vs. t for different R and C

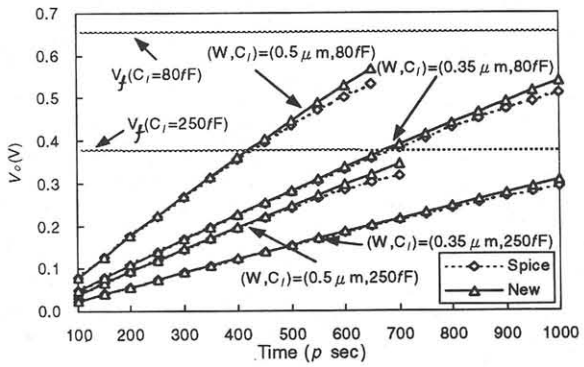

Fig. 2 (b) V_o vs. t for different W and C_l

Fig. 3 demonstrates the percentage error in time domain for given V_o's in terms of percentage of V_f for various values of R, C and C_l. In general, all the errors are less than 4% up to 70% of V_f at V_o. The error at higher V_o is due to the FET entering linear regions.

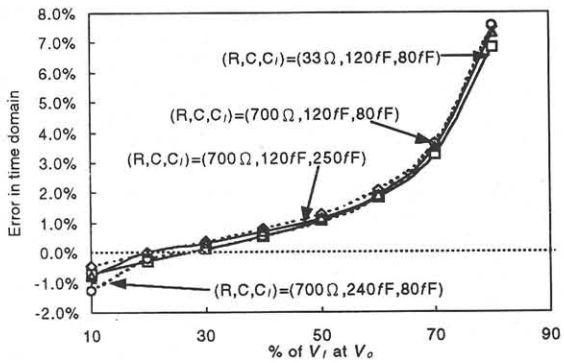

Fig. 3 Percentage error as functions of V_o

Fig. 4 shows the delay time t_d, which is defined as the time when V_o reaches 50% of V_f, as functions of C or C_l. The solid lines generated from the new model are very close to the dotted lines produced by the Spice simulation. Fig. 5 demonstrates the excellent agreement for three initial voltages (V_{ini}) on the bit line. In Fig. 6, the new model agrees pretty well with the simulation at three locations $x=0$, $L/2$ and L for R=1400Ω, C=240fF. Since R and C are higher than the normal ranges, the agreement is much better at low voltages if two terms k=1 and 2 are included.

4. Conclusions

The new analytical delay model for read operation at any locations on DRAM bit lines has been derived. The accuracy is very good for all reasonable resistance, capacitance and initial voltages on the bit line as well as different widths of N-MOSFETs. This new model will be the quick solution for optimization of DRAM circuits and can also be applied to a transmission gate driving another gate through a long wire.

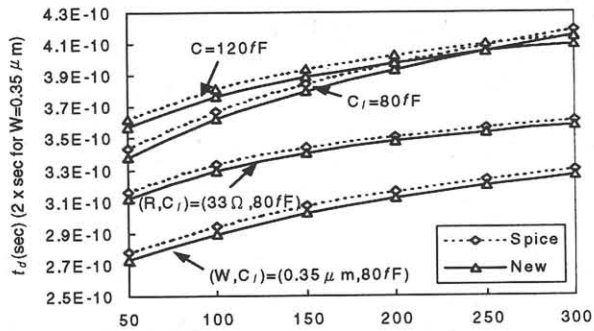

Fig. 4 t_d vs. C or C_l

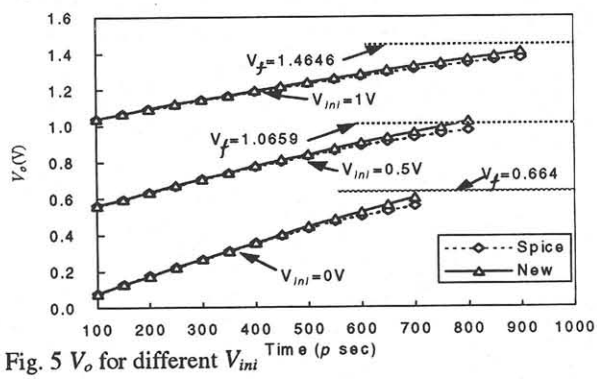

Fig. 5 V_o for different V_{ini}

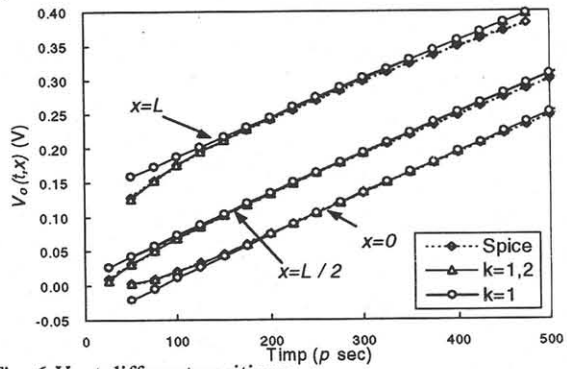

Fig. 6 V_o at different positions

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