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Scaling Law for Secondary Cosmic-Ray Neutron-Induced Soft-Errors in DRAMs

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We examined the scaling law as it applies to secondary cosmic-ray neutron-induced soft-errors via accelerated measurements. The soft-error rates per chip remain constant with advances in DRAM density-generation. However, multiple bit errors will significantly increase with further down-scaling. Consequently, special care should be taken in designing the ECC for future DRAMs.

1. Introduction

The alpha-particle-induced soft-error phenomena have been investigated ever since their well-known discovery in 16kbit DRAMs [1]. Fortunately, the phenomena have been rendered as negligible in recent DRAMs because the charges collected into the storage capacitance decreases with the down-scaling of the device size [2]. On the other hand, secondary cosmic-ray neutrons can generate about ten times as many charges as alpha-particles. These charges are generated along the tracks of various kinds of ions that are produced by reactions between neutrons and silicon nuclei (Fig. 1). It has been reported that system soft-error rates are proportional to the neutron flux, which depends on the location and shielding effects [3, 4]. This suggests that secondary cosmic-ray neutrons are the main contributor of the soft-error phenomena in recent DRAMs. The absolute values of neutron-induced soft-error rates have been reported on preciously [5, 6].

A study of the scaling law of neutron-induced soft-error rates is thus necessary to design reliable DRAMs. With increases in DRAM density-generation, the decreased stored charges and increased bit-density increases the soft-error rate per chip, while the decreased collected charge decreases this rate. Although neutron-induced soft-error rates seem to decrease significantly until 4Mbit DRAMs [7], they seem to increase slightly afterwards [4]. However, the scaling law can not be clearly understood because the device parameters are not shown in past studies.

To clarify the scaling law, we measured the accelerated soft-error rates of 16Mbit DRAMs having various cell areas. We also investigated the characteristics of multiple bit errors to facilitate the design of the ECC (Error Correction Code). We could then predict the reliability of future DRAMs in regard to secondary cosmic-ray neutrons.

2. Experiment

We conducted accelerated measurements at the LANSCE (Los Alamos Neutron Science Center), which has a neutron energy spectrum similar to that found at ground level (Fig. 2) [8, 9]. The chips measured were Fujitsu 16Mbit DRAMs of various cell areas but all having similar process technologies. A few hundred soft-errors were detected in each measurement.

3. Scaling Law of Neutron-Induced Soft-Errors

The neutron-induced soft-error rate (SER) is defined as the number of error bits measured with the same amount of the exposed neutrons. Higher (ALL-1) and lower voltages (ALL-0) for all row and column addresses were applied at the data terminals of DRAM chips.

Figure 3 shows SERs for the various cell areas when the same power supply voltage was applied. As the cell area decreases, the SER decreases because of the lower collected charge. We found a clear relationship between the cell area and SERs when the process technologies employed are quite similar. If the cell area is scaled down by 50%, SERs decrease by a factor of eight. Figure 4 shows SERs as a function of the power supply voltages. As the power supply voltage decreases, the SER increases because of the decreased stored charge. If the voltage is decreased to 2.5 V, the SER increases about two-fold. The decrease of the power supply voltage also equals the decrease of the storage capacitance. Therefore, SERs do not depend significantly on the storage capacitance.

The scaling law for SERs is summarized in Table 1. The effects of the power supply voltage and bit number are compensated for by the effect of the cell area size. Therefore, even if the storage capacitance slightly decreases, the neutron-induced SERs will remain almost constant with advances in DRAM density-generation.

4. Characteristics of Multiple Bit Errors

An ECC is used to suppress soft-errors in high-reliability computer systems. A SCE (Single bit Error Correction) type ECC, however, cannot correct certain multiple bit errors which occur in the same logical addresses. To examine the characteristics of multiple bit errors, all of the storage nodes were set to higher voltages during the measurement. The left side of Figure 5 shows

the multiple bit error patterns for the physical storage nodes. The ratio of each multiple bit error event vs. the total soft-error events is also shown in Figure 5 as a function of the distance between the storage nodes in which soft-errors occur. The multiple bit error events increase significantly as the storage distance decreases. If the storage nodes in Figure 5 have the same logical addresses, its vertical axis corresponds to the ratio of the soft-error events, which cannot be corrected with an ECC, to the total soft-error events. Neutron-induced SERs while employing an ECC will thus clearly increase with advances in DRAM density-generation. Consequently, special care should be taken when designing ECCs for future DRAMs

5. Summary

We examined the scaling law of secondary cosmic-ray neutron-induced soft-errors with accelerated measurements. The SERs per chip have remained constant with advances in DRAM density-generation. However, multiple bit errors will significantly increase as a results of down-scaling. This suggests that special care should be needed in designing the ECCs for future DRAMs.

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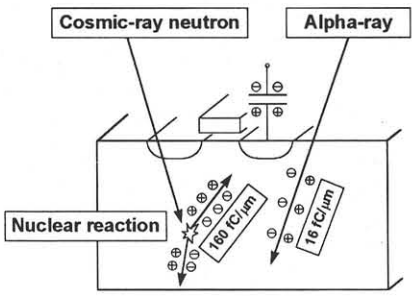

Fig. 1. Alpha and neutron-induced soft error phenomena.

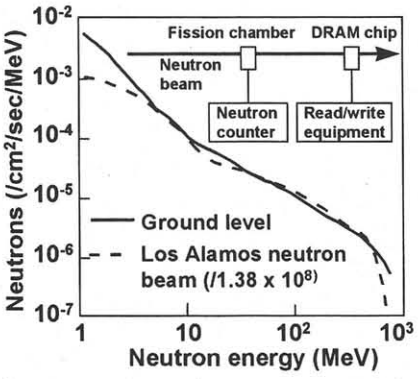

Fig. 2. Accelerated measurements [8].

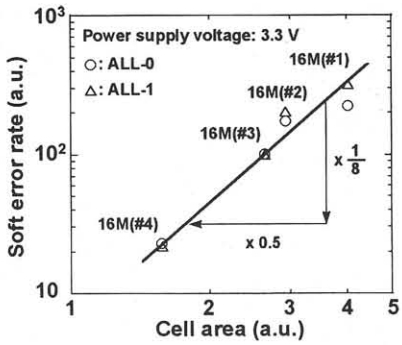

Fig. 3. Soft-error rates for the various unit cell areas.

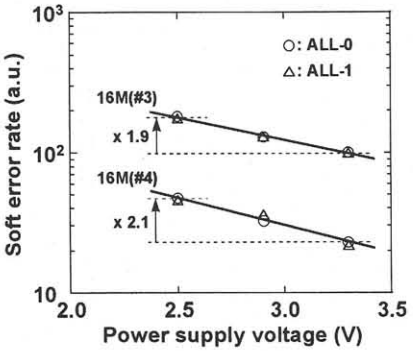

Fig. 4 Soft-error rates as a function of the power supply voltage.

Table 1. Scaling law of neutron induced-soft error rates.

Factor forward next generation		SER
Cell area	x 0.5	x 1/8 (Fig. 3)
Power supply voltage	x 0.7	x 2 (Fig. 4)
Bit number	x 4	x 4
Capacitance	x 1	x 1
SER/chip		x 1

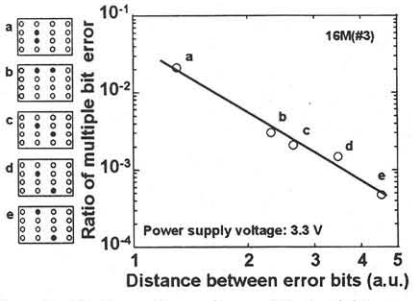

Fig. 5. Ratio of each multiple bit error event vs. the total soft-error events against the distance between the storage nodes in which soft-errors occur.