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A New Merged BiMOS Transistor in an SOI Structure

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1. Introduction

While the shrinkage of MOSFET and reducing supply voltage of CMOS circuits are currently the main stream of LSI device development, merging of bipolar transistor and MOSFET in a circuit such as BiCMOS is very atractive because it offers large fan-out driving ability. The merged circuit is also attracting a great deal of attention from the view point of application to radio frequency (RF) chips. The present merged circuits are fabricated by interconnecting bipolar transistor and MOSFET that are layouted separately and electrically independent each other. If these two are merged in the device level, there appears great advantage in processing speed and packing density. Several bipolar-MOS(BiMOS) merged devices have been proposed using bulk silicon.[1~3] In these device structures, however, problems such as latch-up and insufficient bipolar performance appear.

In this work, we propose a new BiMOS merged transistor structure using an SOI structure. The device can be fully isolated and occupies almost the same area as a MOSFET. Results of simulation and of test fabrication of devices are reported.

2. Device Structure

Figure 1 shows a schematic cross-section of the proposed BiMOS transistor for an n-MOS/pnp-bipolar merged structure. A p-MOS/npn merged structure can be realized by just inverting the conduction type. The structure consists of the frame of a bottom-gate SOI MOSFET. The source and drain contacts are made of poly-Si. In order to realize the bipolar operation mechanism, the source and drain poly-Si contacts are doped with different type of dopants, i.e., the source poly-Si contact is doped to be n^+, and the drain poly-Si contact is doped to be p^+, as a result, a pnp bipolar transistor is built at the drain region of the MOSFET. The p^+ poly-Si at the drain is used as the emitter and the collector can be placed at the top of the device. By using this structure we can avoid a sacrifice in bipolar current gain, which usually appear in a merged bulk device, since the doping profiles can be set as a bipolar device requires.

The n-MOS/pnp device (Fig. 1) and p-MOS/npn device can be used as the pull-down and the pull-up devices, respectively, to form a C-BiCMOS inverter . One advantage of the proposed device is that collector capacitance and collector series resistance can be minimized since the collector can be formed on the top of the device region. Also bipolar mechanism will increase the current drive, in particular, at the linear region of the MOSFET operation. These are particulary useful for high speed operation.

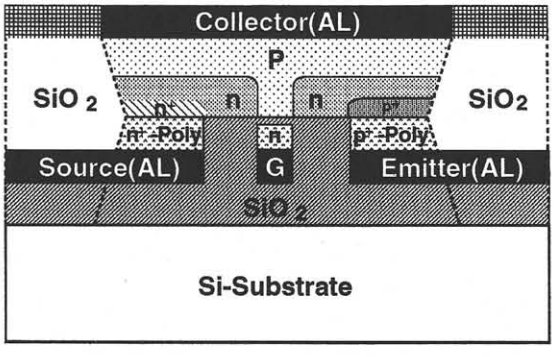

Figure 1: Schematic cross-section of the proposed SOI-BiMOS transistor structure.

3. Simulation

We have analyzed the proposed BiMOS transistor by two dimensional simulation. Device parameters used in the analysis are as follow: W/L=1μm/2μm, gate oxide t_{ox}=300nm, offset length from the edge of base-emitter junction to the interface of drain-channel region = 4μm, impurity concentration in the active region = $2\times10^{16}/cm^3$, thickness of the collector region = 3μm, the dose for the source and the drain/base for merged BiMOS transistor is $2\times10^{14}/cm^2$. For comparison, the operation of the MOSFET having the same dimension was also simulated.

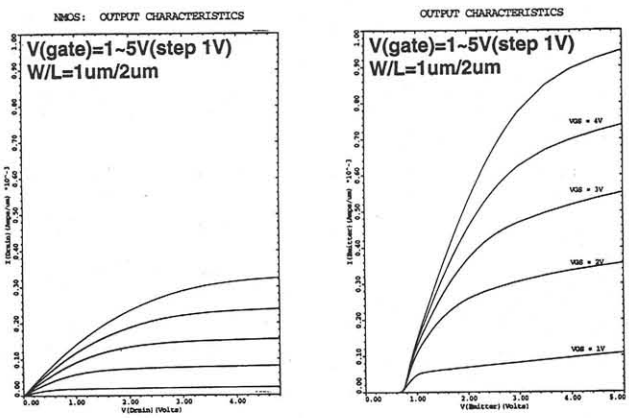

Figure 2: Simulated output characteristics. (a) Conventional nMOSFET, (b) Merged BiMOS transistor.

Figure 2 shows the simulated output characteristic of the proposed n-MOS/pnp BiMOS transistor together with that of the conventional MOSFET. We can see that, The MOSFET current is amplified with the bipolar mechanism. In particular, the drain conductance dI_D/dV_{DS} in the linear region of BiMOS structure is larger than that of conventional nMOS. Although there exist a voltage loss due to the diffusion potential. The improvement in drain conductance is about three times at V_{GS}=5V. This value is nearly equal to the current gain of the bipolar part. The p-MOS/npn device has also been found to operate, as we expect, with higher current drive than the above. Figure 3 shows the subthreshold characteristics of merged n-MOS/pnp BiMOS device. In a merged device, the off-current becomes large because the leakage current of MOSFET is amplified and the source of leakage increases. In fact simulation has shown a larger off current for the merged device than for a MOSFET. The characteristic shown in Fig. 3, however, indicates that the leakage current is sufficiently low for circuit application. The analysis has also shown that the subthreshold slop is improved in the merged structure by optimizing the device parameters.

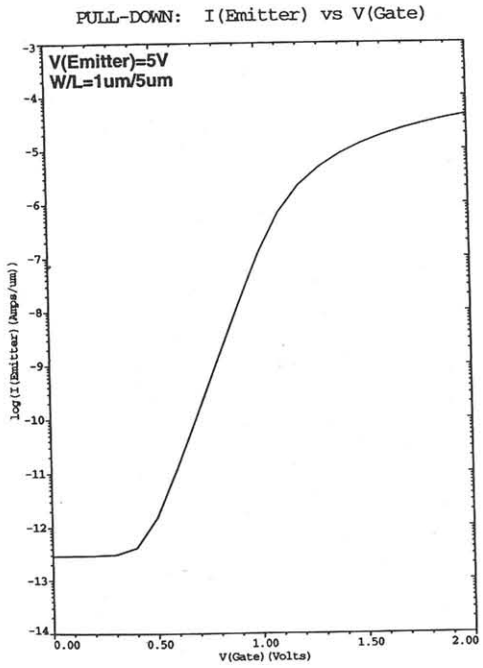

Figure 3: Simulated subthreshold characteristic.

4. Experimantal

We have fabricated a test device by using a wafer bonding and polishing technique. That is, the MOSFET structure having p^+-poly-Si at the drain was formed on a bulk silicon wafer, followed by bonding to another wafer in face-to-face. The bonded wafer was then mechanically and chemically polished until the LOCOS oxide appears and the active region is fully isolated. Finally the collector electrode was formed on the active island region. Photomasks used were a set that designed for a conventional MOS device.

Figure 5 shows the I_E-V_{ES} characteristics. The characteristic that corresponds to the linear region of the MOSFET was ploted in the figure. The characteristic observed for a MOSFET having the same device structure was also shown in figure. We can see that the current drive is very much improved in the merged device. The large off current observed in Fig. 5(b) for the merged device is expected to be suppressed by MOSFET channel doping.

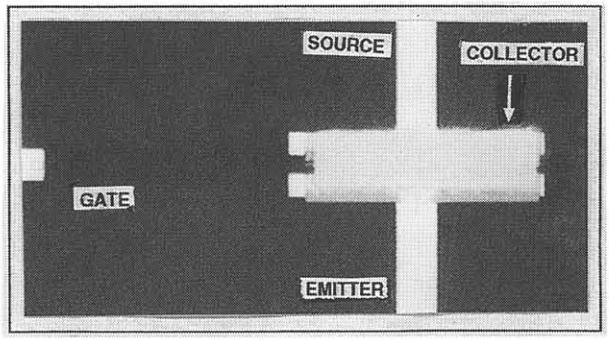

Figure 4: Photo of a test device.

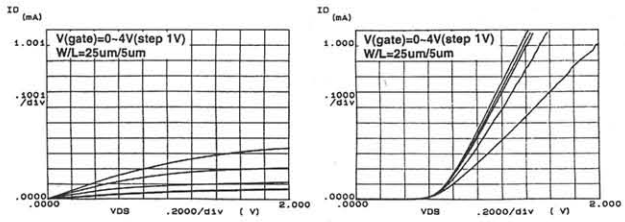

Figure 5: Output characteristic in linear region. (a): conventional nMOSFET. (b): merged BiMOS transistor.

5. Conclusion

A new MOS/bipolar merged device on a SOI structure has been proposed. The full-isolation ability of SOI makes it possible to merge MOS and bipolar without the latch-up problem and a sacrifice of device performance. Simulation has shown that the high current drive and sufficient switching behavior. Test fabrication using a MOS process has shown the feasibility of the device.

References

1) S. Shibata: Japan Patent, No. S56-100461, p. 255. [in Japanese].
2) M. Fujishima, K. Asada, T. Sugano: IEICE Trans. Vol **J72-C-II** (1989) p. 1171. [in Japanese].
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