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A Precise SOI Film Thickness Measurement Including Gate Depletion and Quantum Effects

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1. Introduction

In FD (fully depleted) SOI devices, the SOI film thickness t_{SOI} is the key parameter that affects transistor characteristics such as threshold voltage V_T [1] and source/drain parasitic resistance R_{SD}. A C-V method [2] is widely used to measure t_{SOI}, because this can directly measure t_{SOI} without destroying samples.

However, the C-V method contains an unknown measurement error : the value of t_{SOI} measured by the C-V method is 4–5 nm thinner than that by TEM observation. This difference becomes fatal when the t_{SOI} is scaled down.

In this report, we show that the gate depletion thickness and the inversion layer thickness are essential to explain the difference between the C-V method and the TEM observation. By introducing these values in a conventional C-V method, a precise SOI thickness measurement is demonstrated.

2. SOI film thickness measurement

Figure 1 shows the setup for the SOI film thickness measurement. The capacitance between the gate and the source/drain is measured with two different back-gate biases V_{BG}. Figure 2 shows the C-V measurement result. The SOI film capacitance C_{SOI} in the body region is described using the following equation [2] :

$$1/C_{SOI} = 1/(C_{MIN} - C_{PARA}) - 1/(C_{MAX} - C_{PARA}), \quad (1)$$

where C_{MAX} is C_g in the inversion region with $V_{BG} = 0$ V, C_{MIN} is C_g in the accumulation region with $V_{BG} = 30$ V, and C_{PARA} is the parasitic capacitance such as the gate overlap and the fringe capacitance. In the conventional method, the SOI film thickness t_{SOI} can be obtained from the Eq. (1).

However, the SOI film thickness given by this measurement (Fig. 2) is 4.1 nm thinner than that given by the TEM observation (Fig. 3). We assume that both the inversion layer thickness [3] and the gate depletion thickness can not be ignored for the C-V measurement, especially when the SOI film thickness is less than 50 nm. The following are new definitions of the C-V measurement.

a). Strong inversion region with V_{BG}=0 V (Fig. 4)

The capacitance C_{MAX} is described as a series of the gate oxide capacitance C_{OX}, the front-gate inversion layer capacitance C^F_{INV}, and the gate depletion capacitance C_{DEP} :

$$1/C_{MAX} = 1/C_{OX} + 1/C^F_{INV} + 1/C_{DEP} \quad (C_{PARA} << C_{MAX}). \quad (2)$$

b). Accumulation region with V_{BG}=30 V (Fig. 5)

The capacitance C_{MIN} is described as a series of the gate oxide capacitance C_{OX}, the SOI film capacitance C_{SOI}, and the back-gate inversion layer capacitance C^B_{INV} :

$$1/C_{MIN} = 1/C_{SOI} + 1/C_{OX} - 1/C^B_{INV} \quad (C_{PARA} << C_{MIN}). \quad (3)$$

Using Eqs. (2) and (3), t_{SOI} can be written as

$$t_{SOI} = \varepsilon_{Si} WL(C_{MAX} - C_{MIN}) / C_{MAX}C_{MIN} + t^F_{INV} + t^B_{INV} + t_{DEP}, \quad (4)$$

where L is the gate length, W is the gate width and t^F_{INV} and t^B_{INV} are the front and back gate inversion layer thickness, t_{DEP} is the gate depletion thickness and ε_{Si} is the dielectric constant of silicon.

3. Experiments

Samples are nMOSFETs (whose gate length is 50 μm and gate width is 50 μm, t_{OX} is 8 nm) on a low-dose SIMOX wafer (buried oxide layer is 110 nm).

The inversion layer thickness t^F_{INV} and t^B_{INV} are obtained from the simulated electron concentration as a function of depth into the silicon substrate by using a self-consistent calculation of both Poisson's and Schrödinger's equations taking the quantum effects (Fig. 6). From this simulation, the thickness of the inversion layer t^F_{INV} is 1.2 nm (front-gate oxide is 8 nm, gate bias is 3 V) and t^B_{INV} is 1.3 nm (buried oxide thickness is 110 nm, back-gate bias is 30 V).

To obtain t_{DEP}, we used the bulk MOSFET fabricated simultaneously. The gate depletion capacitance C_{DEP} can be measured from the difference between the capacitance in the accumulation region and the inversion region (Fig. 7). From the capacitance C_{DEP}, t_{DEP} is estimated to be 1.92 nm. Finally, Eq. (4) can be rewritten as

$$t_{SOI} = \varepsilon_{Si} WL(C_{MAX} - C_{MIN}) / C_{MAX}C_{MIN} + 4.42 \text{ nm}. \quad (5)$$

For comparison, we measured the SOI film thickness using a TEM photograph with the same MOSFETs shown in Fig. 8. The SOI thickness using Eq. (5) shows better agreement with that by TEM observation. This indicates that the gate depletion and the inversion layer thickness cause the difference in the measurement of the SOI film thickness between the C-V method and TEM observation.

Figure 9 shows the distribution of the SOI film thickness in a 6-inch wafer using this work. The V_T variation corresponding to ±2.8 nm of the t_{SOI} variation is ±0.037 V (Fig. 10).

4. Conclusions

A precise SOI thickness measurement is demonstrated by introducing the gate depletion and the inversion layer thickness in a conventional C-V method. This method has much potential in characterizing a FD device with a very thin SOI film.

References

[1] H.-K. Lim and J.G. Fossum, IEEE Trans. on Electron Dev., p. 1244, 1983.
[2] J. Chen *et al.*, IEEE Electron Device Lett., Vol. 12, No. 8, p. 453, Aug. 1991.
[3] Y. Ohkura, Solid - State Electron, Vol. 33, No. 12, p.1581, 1990.

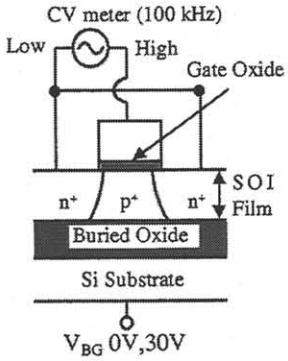


Fig. 1 CV measurement setup for SOI-MOSFET

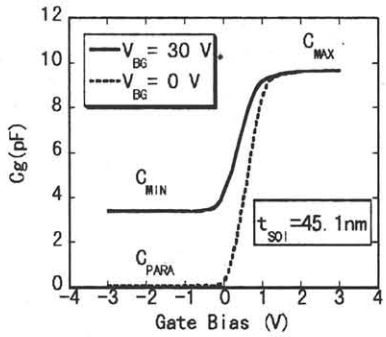


Fig. 2 C-V measurement result (t_{OX}= 8 nm, W/L=50/50 μ m)

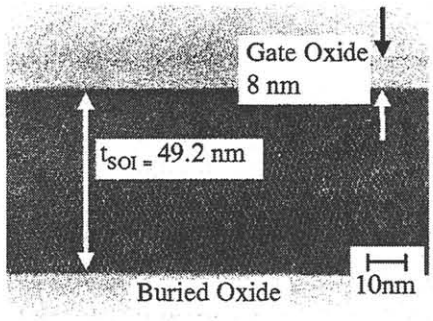
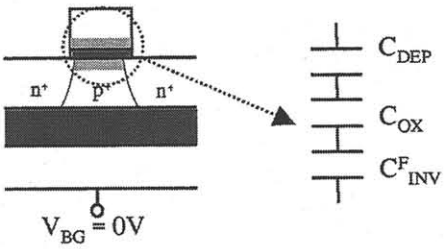
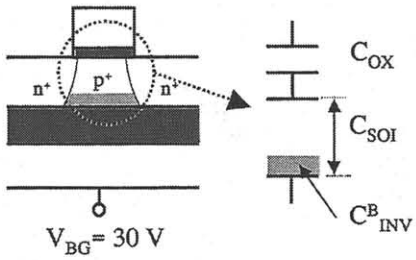


Fig. 3 Cross-sectional TEM image of SOI film



$$1/C_{MAX} = 1/C_{OX} + 1/C^{F}_{INV} + 1/C_{DEP}$$
$$(C_{PARA} << C_{MIN})$$

Fig. 4 Strong inversion region with V_{BG} = 0 V



$$1/C_{MIN} = 1/C_{OX} + 1/C_{SOI} - 1/C_{DEP}$$
$$(C_{PARA} << C_{MIN})$$

Fig. 5 Accumulation region with V_{BG} = 30 V

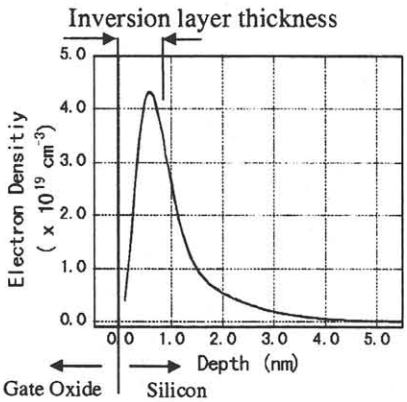


Fig. 6 Simulated electron concentration as a function of depth into silicon substrate. (gate vias 3 V, t_{OX}= 8 nm)

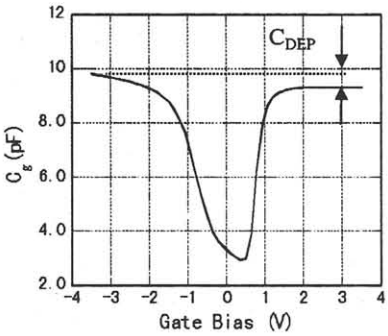


Fig. 7 C-V characteristic of bulk nMOSFET (t_{OX}= 8 nm, W/L=50 μ m/50 μ m)

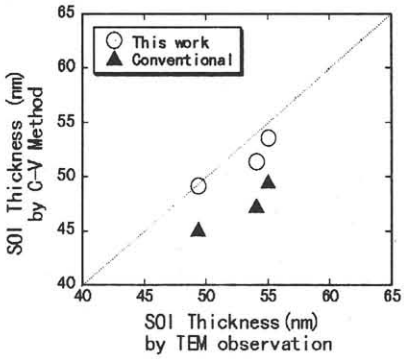


Fig. 8 SOI film thickness taking gate depletion and quantum effect

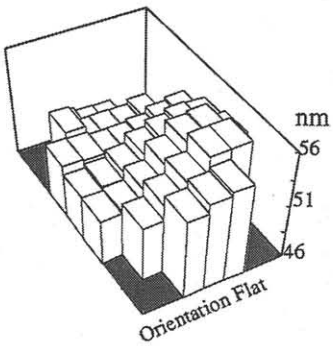


Fig. 9 The distribution of the SOI film thickness in 6-inch wafer

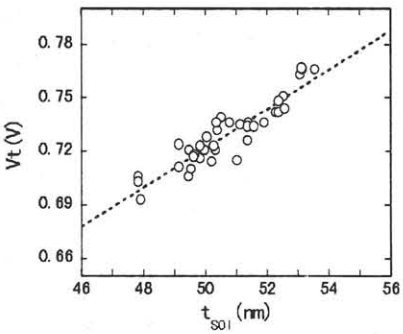


Fig. 10 The dependence of Vt on t_{SOI} (t_{OX}= 8 nm, W/L=50/50 μ m, channel B 70 keV, 5 x 10^{12} $cm^{-2}$for nMOSFET)

The V_T variation corresponding to $\pm$2.8 nm of the t_{SOI} variation is $\pm$0.037 V.